

Compal confidential

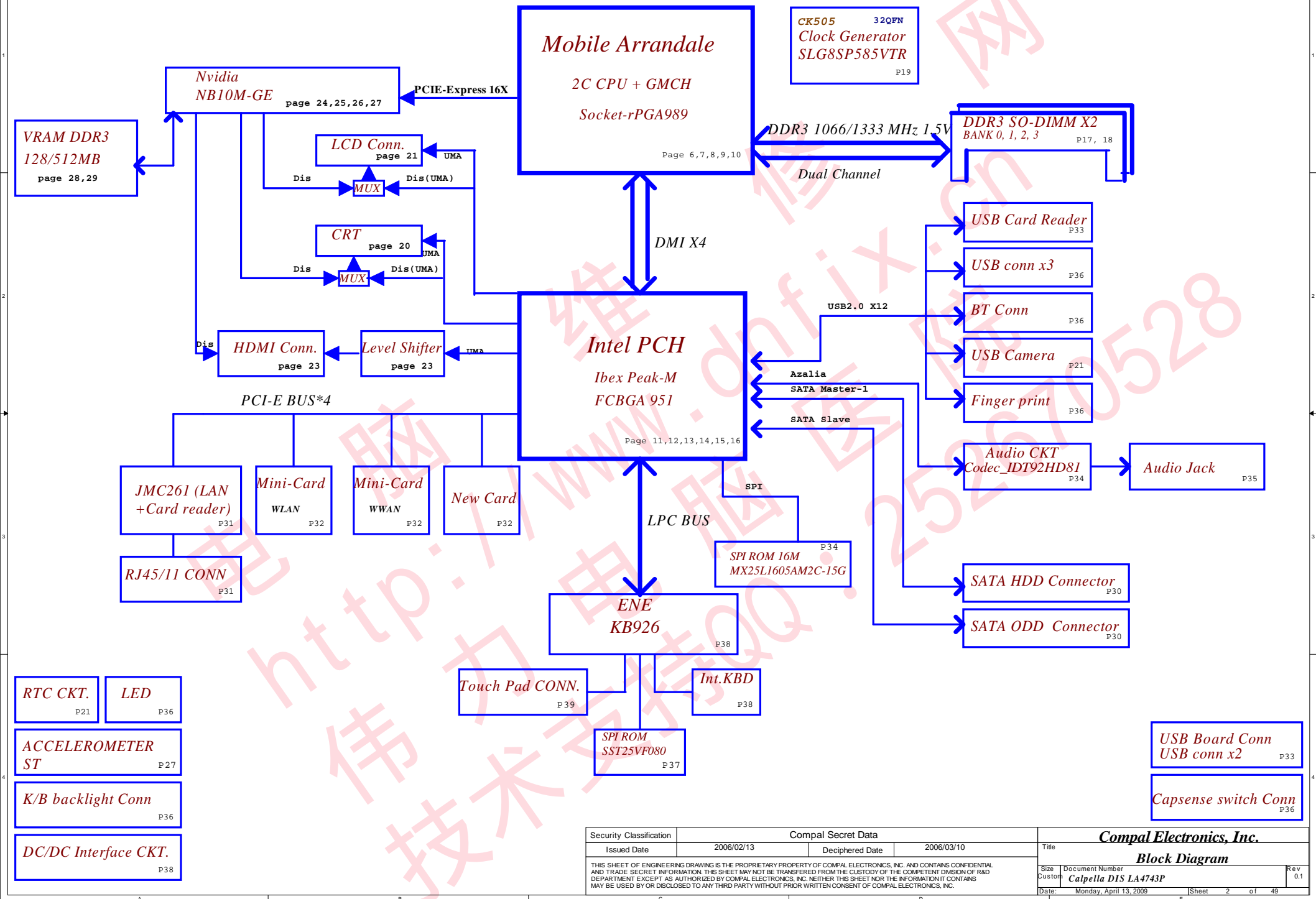
Schematics Document

Mobile Auburndale rPGA989 with
Intel PCH(Ibex Peak-M) core logic

2009-04-13

機 等 密	硬體二部	
	產出人員	
	產出日期	
	解密日期	

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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Title	Block Diagram	
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Voltage Rails

O MEANS ON X MEANS OFF

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +2.5VS +1.8VS
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



: means Digital Ground



: means Analog Ground

@ :	means just reserve , no build
45@ :	means need be mounted when 45 level assy or rework stage.
BATT @ :	means need be mounted when 45 level assy or rework stage.
CONN@ :	means ME part
SG@ :	means stuff when Switchable graphic
UMA@ :	means stuff when UMA skus
VRAM@ :	X76 level
8111DL@ :	Only for Giga LAN
DEBUG@ :	For debug
Cypress@ :	Only For Cypress Capacitor sensor board
ENE@ :	Only For ENE Capacitor sensor board
M3@ :	Only For Intel DDR3 VREF
PA@ :	Only For PA
PR@ :	Only For PR

USB assignment:

USB-0	Right side
USB-1	Right side
USB-2	Left side(with ESATA)
USB-3	X
USB-4	Camera
USB-5	WLAN
USB-6	Bluetooth
USB-7	Finger Printer
USB-8	MiniCard(WWAN/TV)
USB-9	Express card
USB-10	X
USB-11	X

PCIe assignment:

PCIe-1	WWAN
PCIe-2	WLAN
PCIe-3	LAN
PCIe-4	New card
PCIe-5	X
PCIe-6	X

SATA assignment:

SATA0	HDD
SATA1	ODD
SATA2	X
SATA3	X
SATA4	ESATA
SATA5	X

SMBUS Control Table

	SOURCE	XDP	BATT	Thermal Sensor	SODIMM	CLK CHIP	WLAN WWAN	NB10M Thermal Sensor	NB10M-GE	Cap sensor board	NEW CARD	G sensor
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	X	X	X	X	X	X	V	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	X	X	X	X	X	X	X	X
SMBCLK SMBDATA	PCH	V	X	X	V	V	V	X	X	X	V	V
SML0CLK SML0DATA	PCH	X	X	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH	X	X	X	X	X	X	X	X	X	X	X

+3VS +5VL +3VS +3VS +3VALW +5VL +3VALW +3VS

PCH I2C / SMBUS ADDRESSING

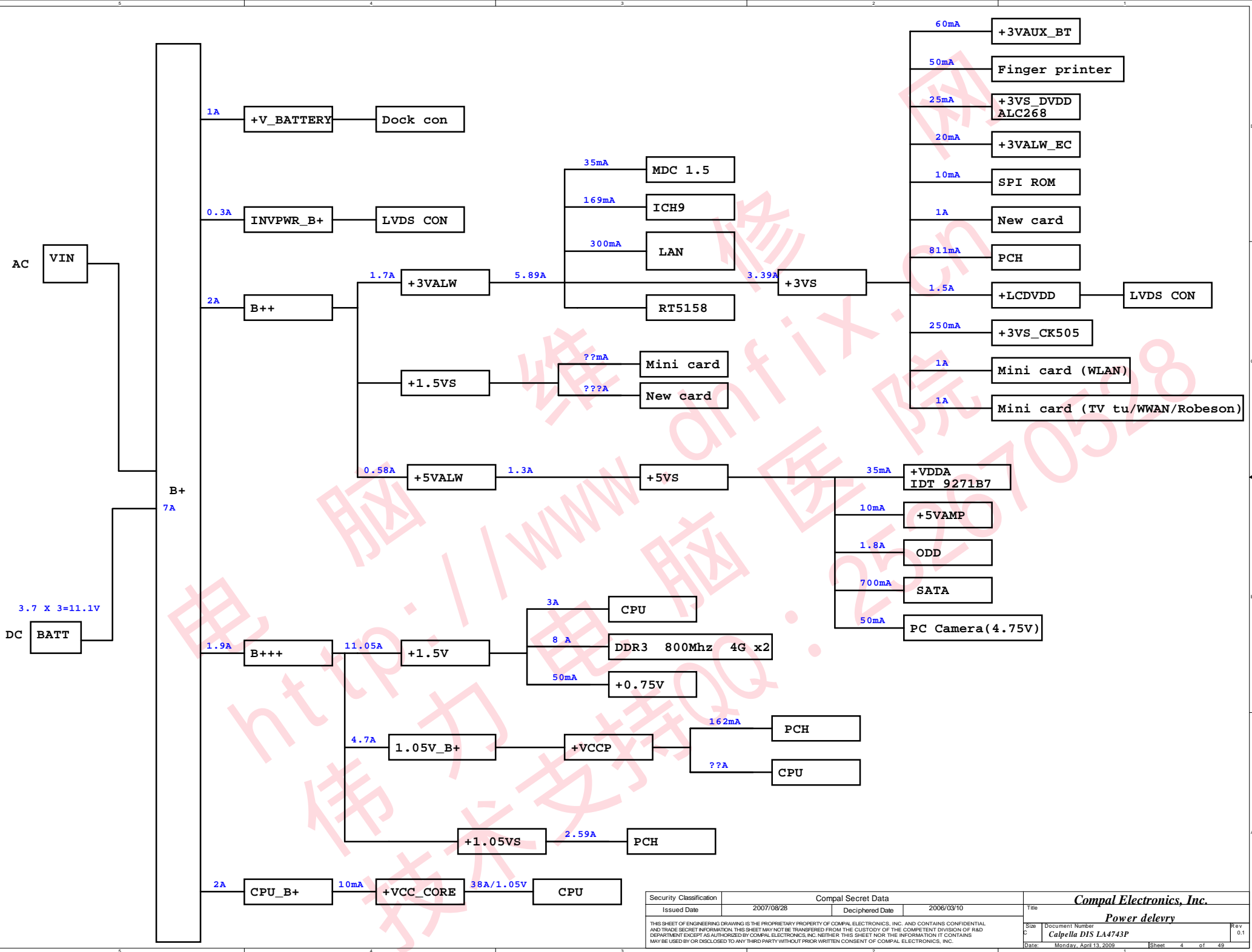
DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

45172932L01 : Switchable graphic
45172932L02 : UMA only

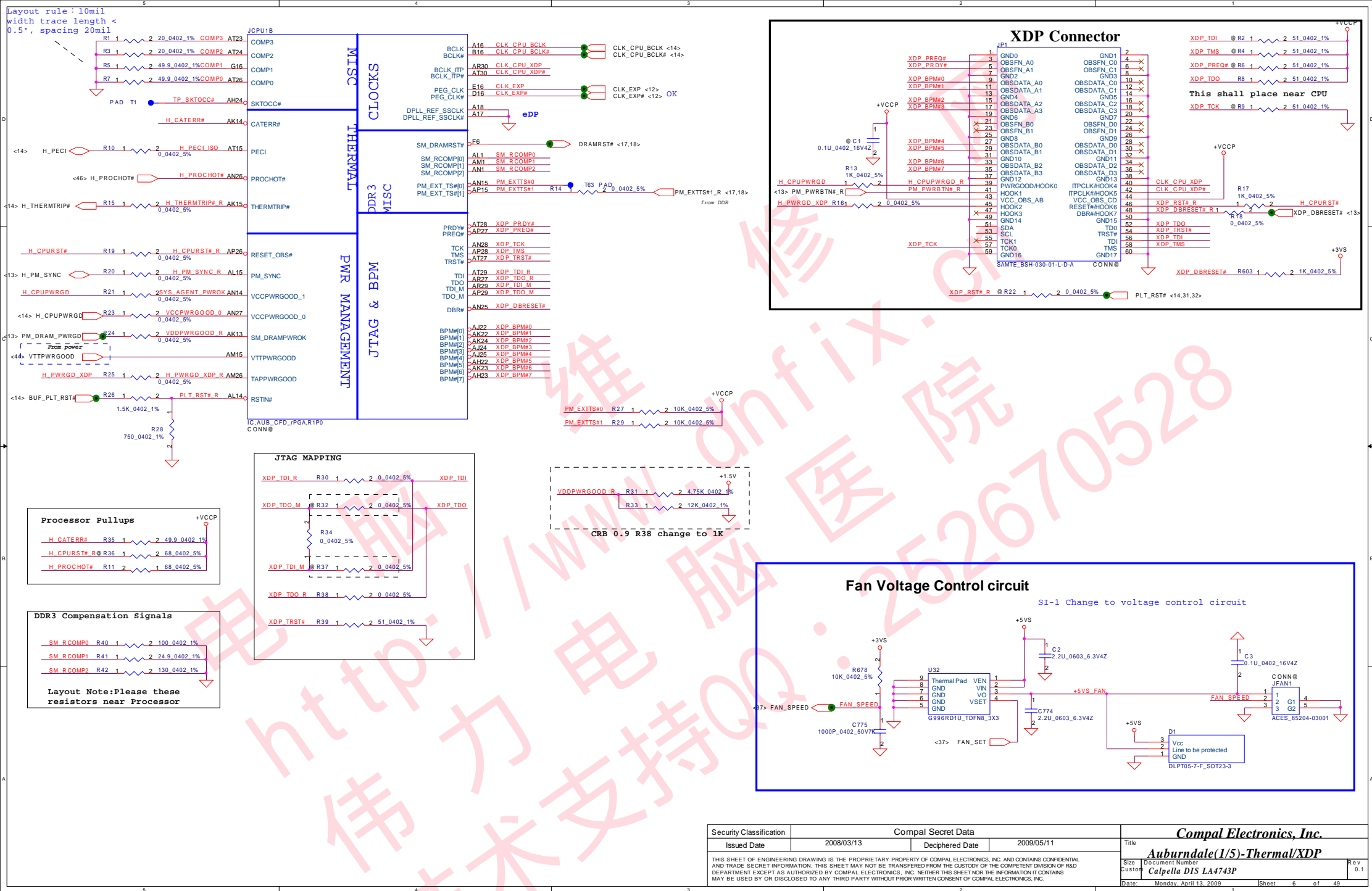
NB10M-GE SMBUS Control Table

	SOURCE	LVDS	CRT	HDMI
D_EDID_DATA D_EDID_CLK	NB10M	V	X	X
D_CRT_DDC_DATA D_CRT_DDC_DATA	NB10M	X	V	X
HDMIDAT_VGA HDMICLK_VGA	NB10M	X	X	V

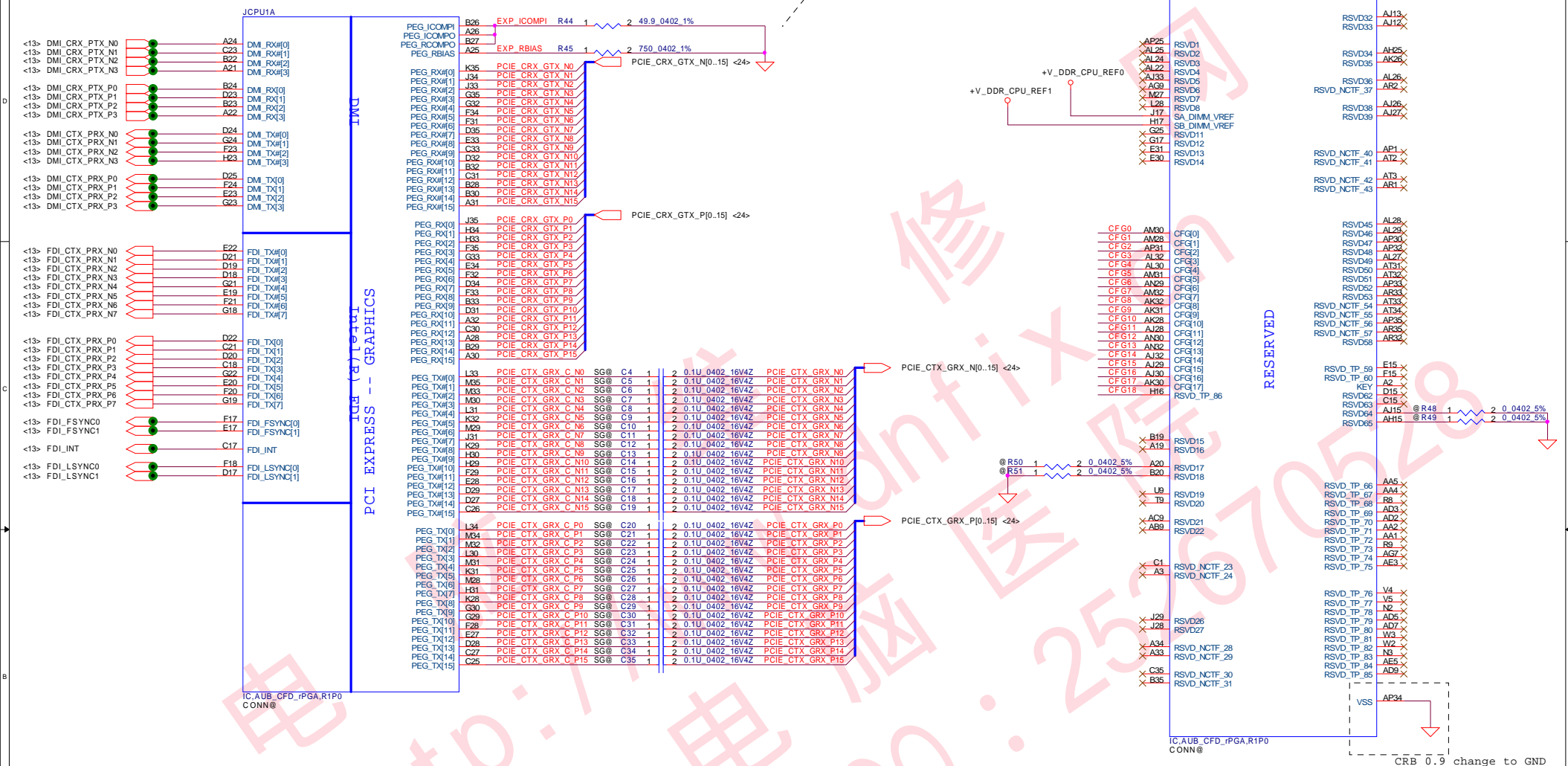
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Calpella Discrete power on sequence				97.09.16.	Spec	define	min	Max
	Vin							
	B+							
	+3VL							
	+5VALW/+3VALW							
EC->PCH	RSMRST#	→ T1 ←			T1, >10ms, +3VALW to RSMRST#	T03	10 ms	-
	ON/OFF#	→ T2 ←			T2, User define			
EC->PCH	PWRBTN_OUT#	→ T3 ←			T3, 150ms, T4, 100ms			
PCH->EC	SLP_S5#	→ T5 ←			T5, >100ms, RSMRST# to SLP_S5#	T07	100 ms	-
PCH->EC	SLP_S4#	→ T6 ←			T6, >30us, SLP_S5# to SLP_S4#	T08	30 us	-
EC->PWR	SYSON	→ T7 ←			T7, 10ms, SLP_S3# to SYSON			
	+1.5V							
PCH->EC	SLP_S3#	→ T8 ←			T8, >30us, SLP_S4# to SLP_S3#	T09	30 us	-
EC->PWR	SUSP#	→ T9 ←			T9, 20ms, SLP_S3# to SUSP#			
	+5VS/+3VS/+1.8VS/+1.5VS/+1.05VS/+VCCP							
PWR->CPU	VTTPWRGOOD	→ T10 ←			T10, VCCP stable to VTTPWRGOOD assertion to the processor	T13	0.0001 ms	500 ms
EC->PWR	VR_ON	→ T11 ←			T11, >130ms, SLP_S3# to VR_ON	T16	99 ms	-
	+CPU_CORE	→ T12 ←			T12, Intel MVP soft start ramp-up time of +VCC_CORE	T17	-	3 ms
PWR->Clock	IMVP_CLK_EN#	→ T13 ←			T13, Duration Intel MVP V-boot, timing set by IMVP6.5	T18	10 us	100 us
	CLKIN_BCLK			Stable				
PWR->PCH or(EC->PCH)	VGATE or(PWROK)	→ T14 ←			T14, CLKIN_BCLK stable to VGATE assertion	T19	1 ms	-
PWR->PCH	PWROK	→ T15 ←			T15, IMVP_CLK_EN# to VGATE assert, Timing set by MVP6.5	T20	3 ms	20 ms
PWR->PCH	SYS_PWROK							
	MEPWROK				MEPWROK connecto to PWROK(IAMT disable)			
	DRAMPWROK	→ T16 ←			T16, +1.5V stable to DRAMPWROK assertion, Timing set by PCH	T22	100 ns	-
	CLKOUT_BCLK	→ T17 ←			T17, VGATE assertion to DRAMPWROK assertion, Timing set by PCH	T23	1 ms	-
PCH->CPU	PROCPWRGD	→ T18 ←			T18, CLKOUT_BCLK stable to VCCPWRGOOD_0 + VCCPWRGOOD_1 assertion to Processor. Timing set by	T24	10 BCKS	-
	VCCPWRGOOD_0	→ T19 ←			T19, VTTPWRGD to VCCPWRGOOD assertion, Timing set by PCH	T25	1 ms	-
	VCCPWRGOOD_1	→ T20 ←			T20, VGATE assertion to VCCPWRGOOD assertion, Timing by PCH	T26	1 ms	100 ms
		→ T21 ←			T21, VCCORE stable to VCCPWRGOOD assertion	T27	0.05 ms	-
PCH->N.C.	SUS_STAT#	→ T22 ←			T22, VCCPWRGOOD to SUS_STAT#, timing default is 1ms	T28	0.03 ms	-
PCH->Device	PLT_RST#	→ T23 ←			T23, SUS_STAT# to PLTRST#, timing set by PCH	T29	60 us	-



Layout rule: trace
length < 0.5"



CFG Straps for PROCESSOR

CFG0 @R52 1 2 3.01K 0402 1%

CFG4 @R53 1 2 3.01K 0402 1%

PCI-Express Configuration Select
CFG0
1: Single PEG
0: Bifurcation enabled

CFG4-Display Port Presence
CFG4
1: Disabled; No Physical
Display Port
0: Enabled; An external
Display Port
device is connected to the
Embedded Display Port

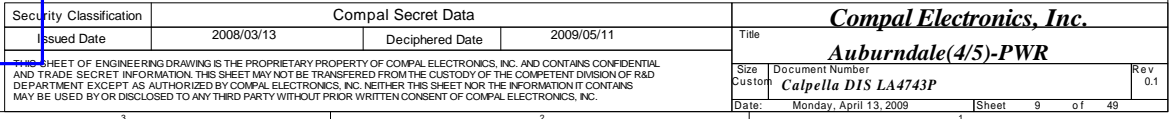
CFG3 @R54 1 2 3.01K 0402 1%

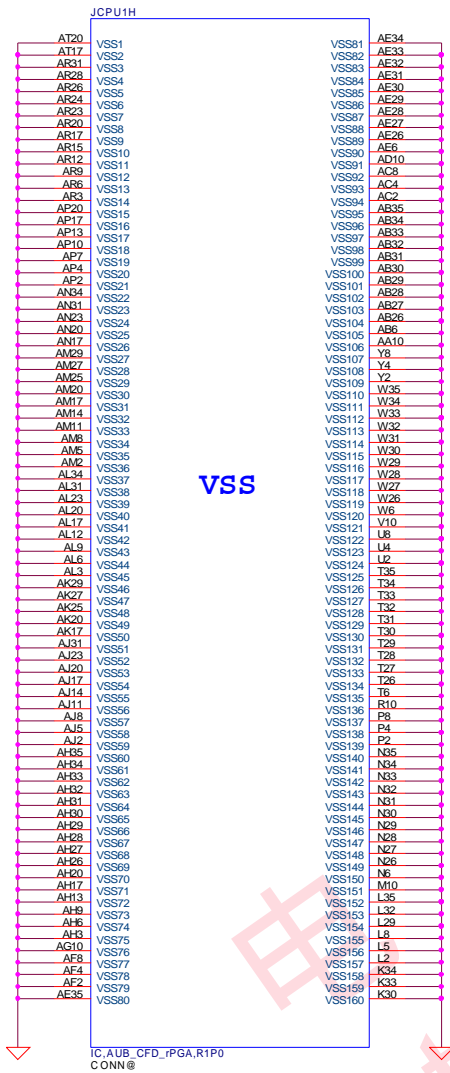
CFG3-PCI Express Static Lane Reversal
CFG3
1: Normal Operation
0: Lane Numbers Reversed
15 -> 0, 14 -> 1,

CFG7 @R55 1 2 3.01K 0402 1%
Only temporary for early
CFD samples (rPGA/BGA)
Only for pre ESI sample

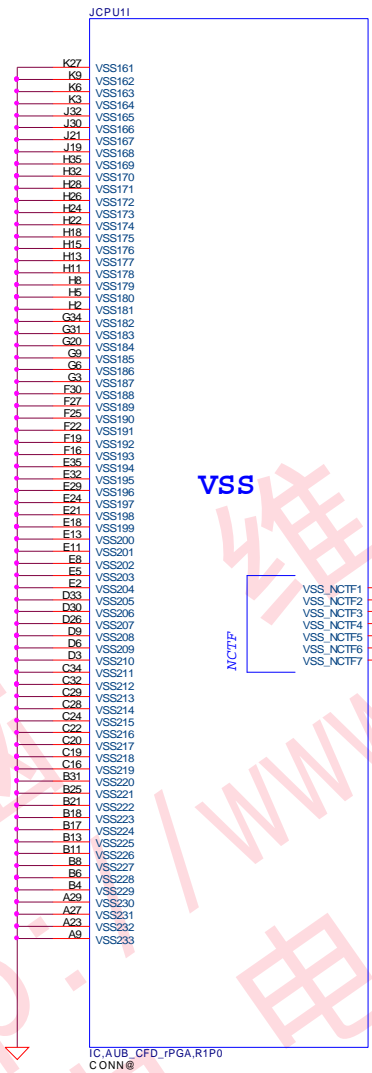
CFG7
WW33GPD 3.01K on CFG7 for PCIE Jitter
WW41: don't staff

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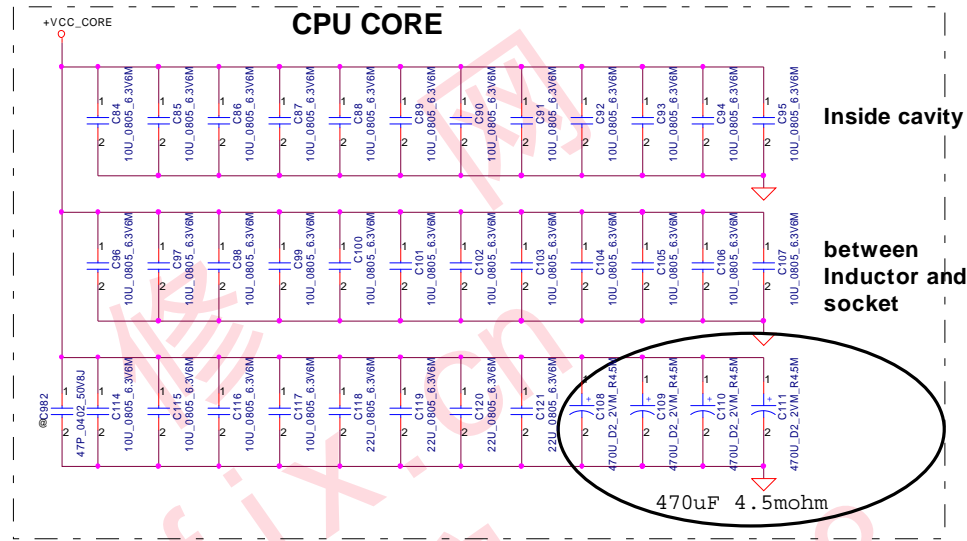
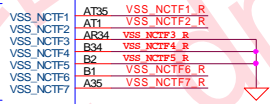


VSS

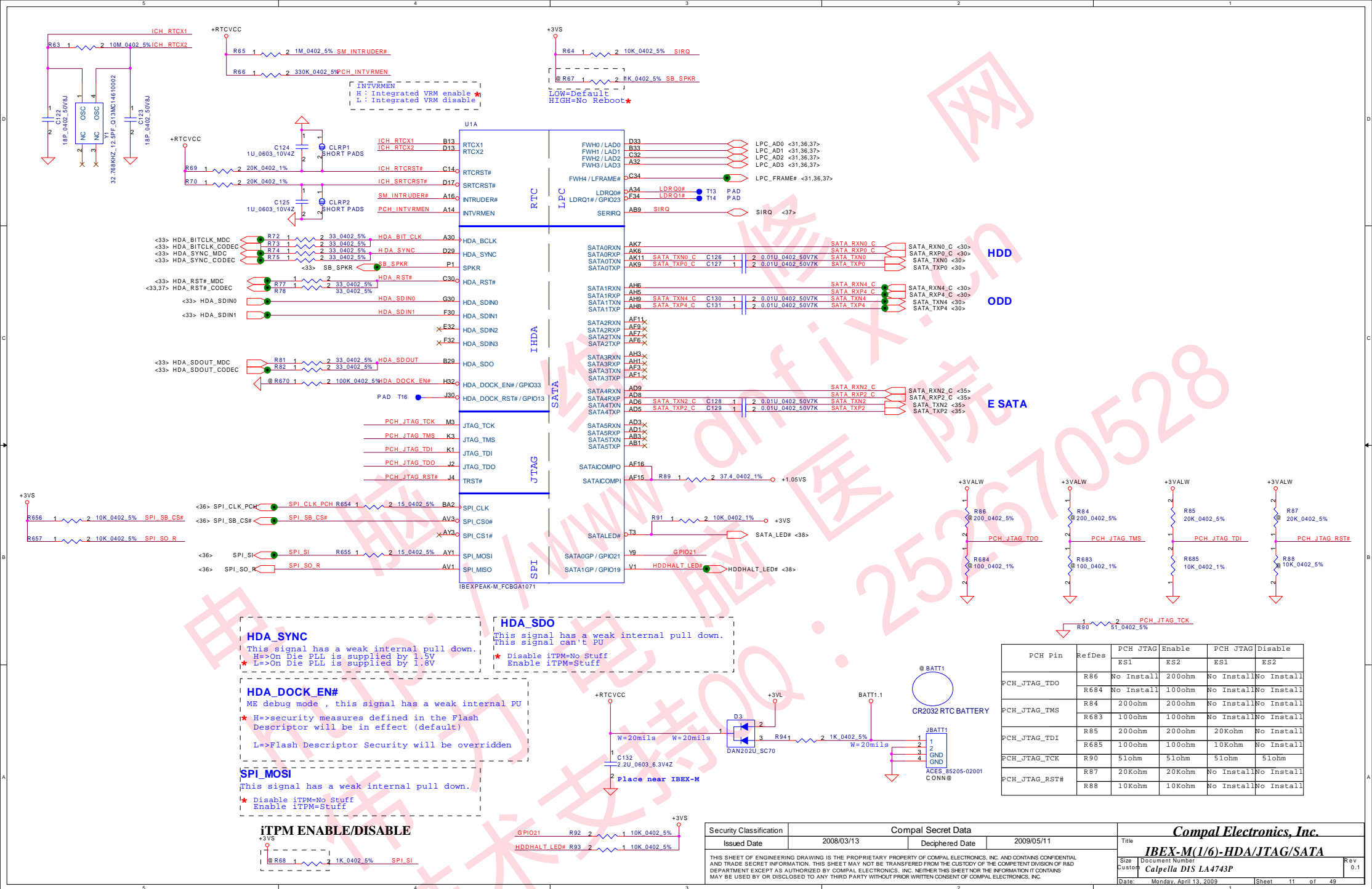


VSS

NCTF

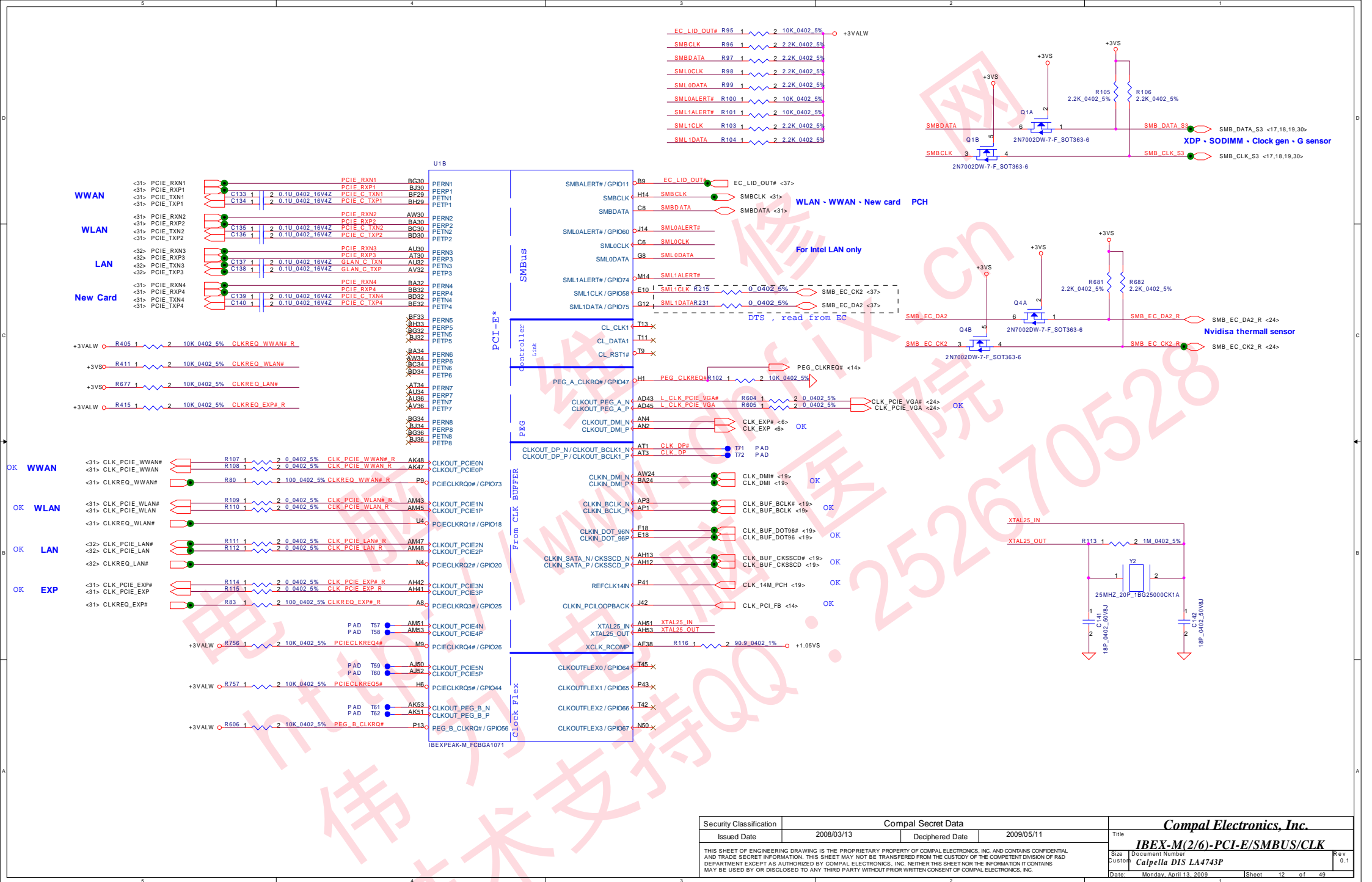


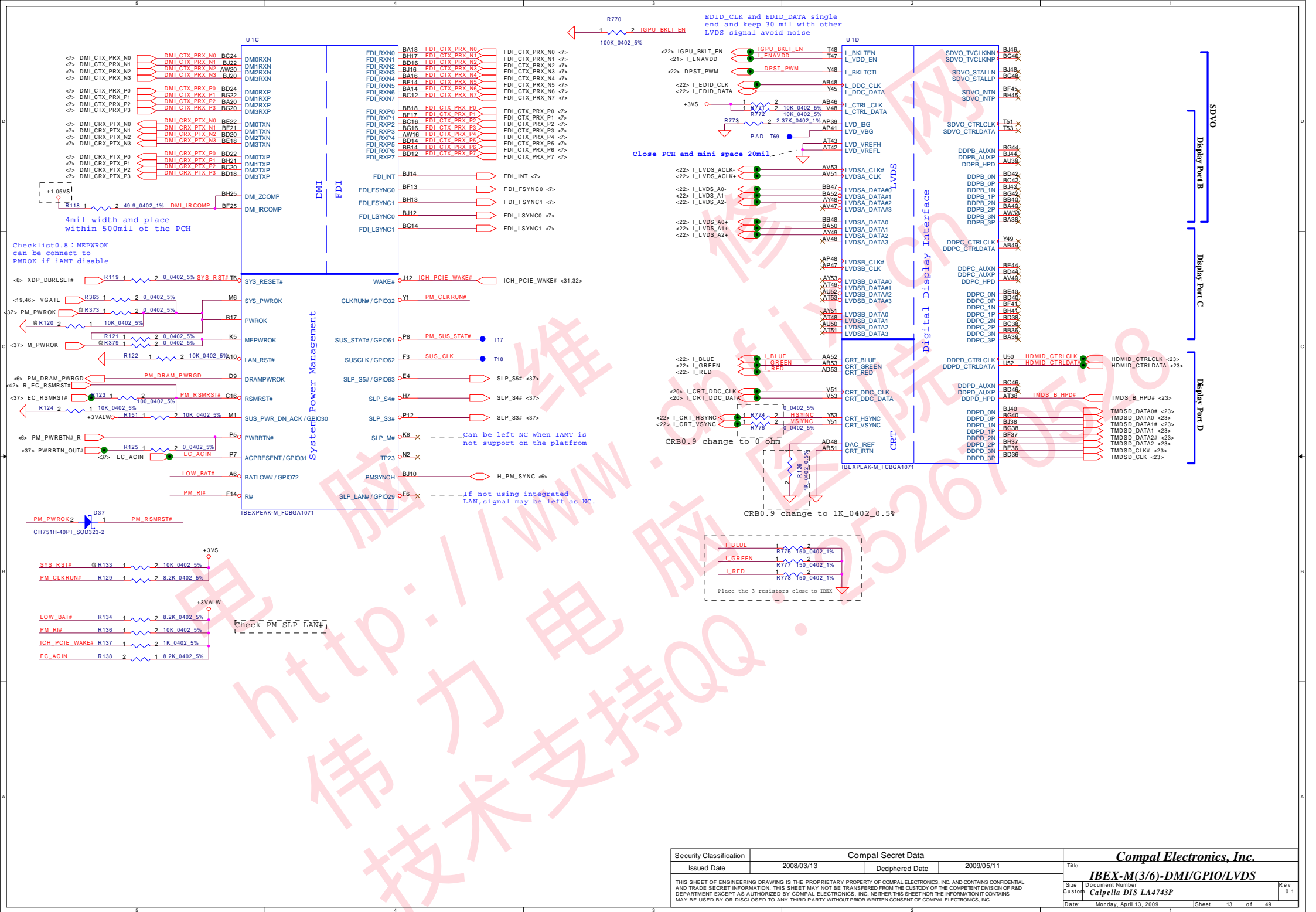
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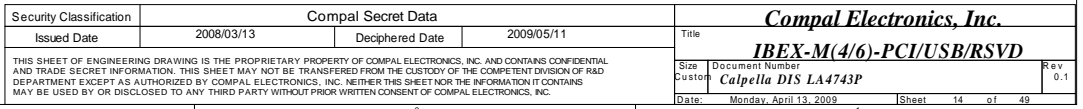


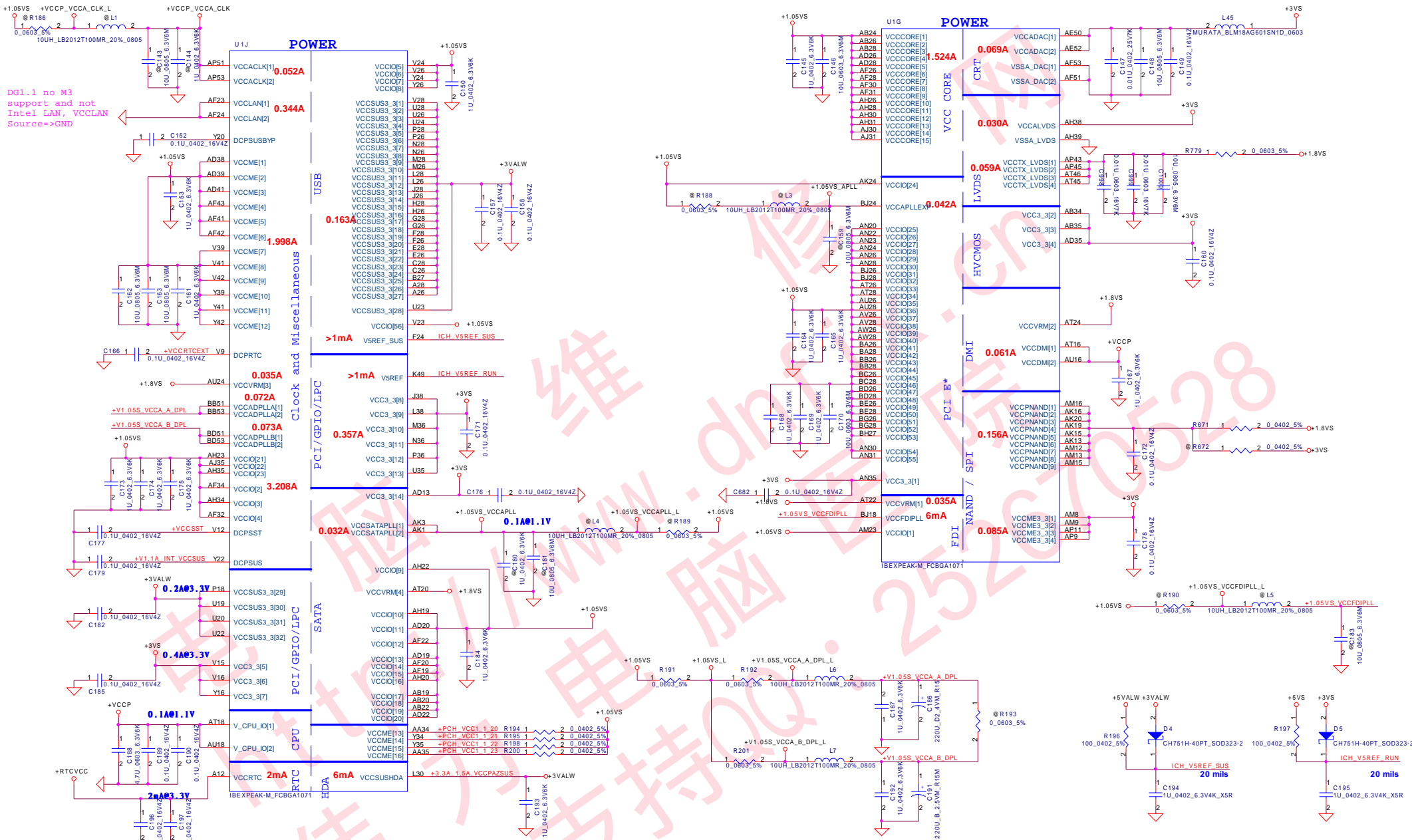
PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R86	No Install	200ohm	No Install	No Install
	R684	No Install	100ohm	No Install	No Install
PCH_JTAG_TMS	R84	200ohm	200ohm	No Install	No Install
	R683	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDI	R85	200ohm	200ohm	20kohm	No Install
	R685	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R90	51ohm	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R87	20Kohm	20Kohm	No Install	No Install
	R88	10Kohm	10Kohm	No Install	No Install

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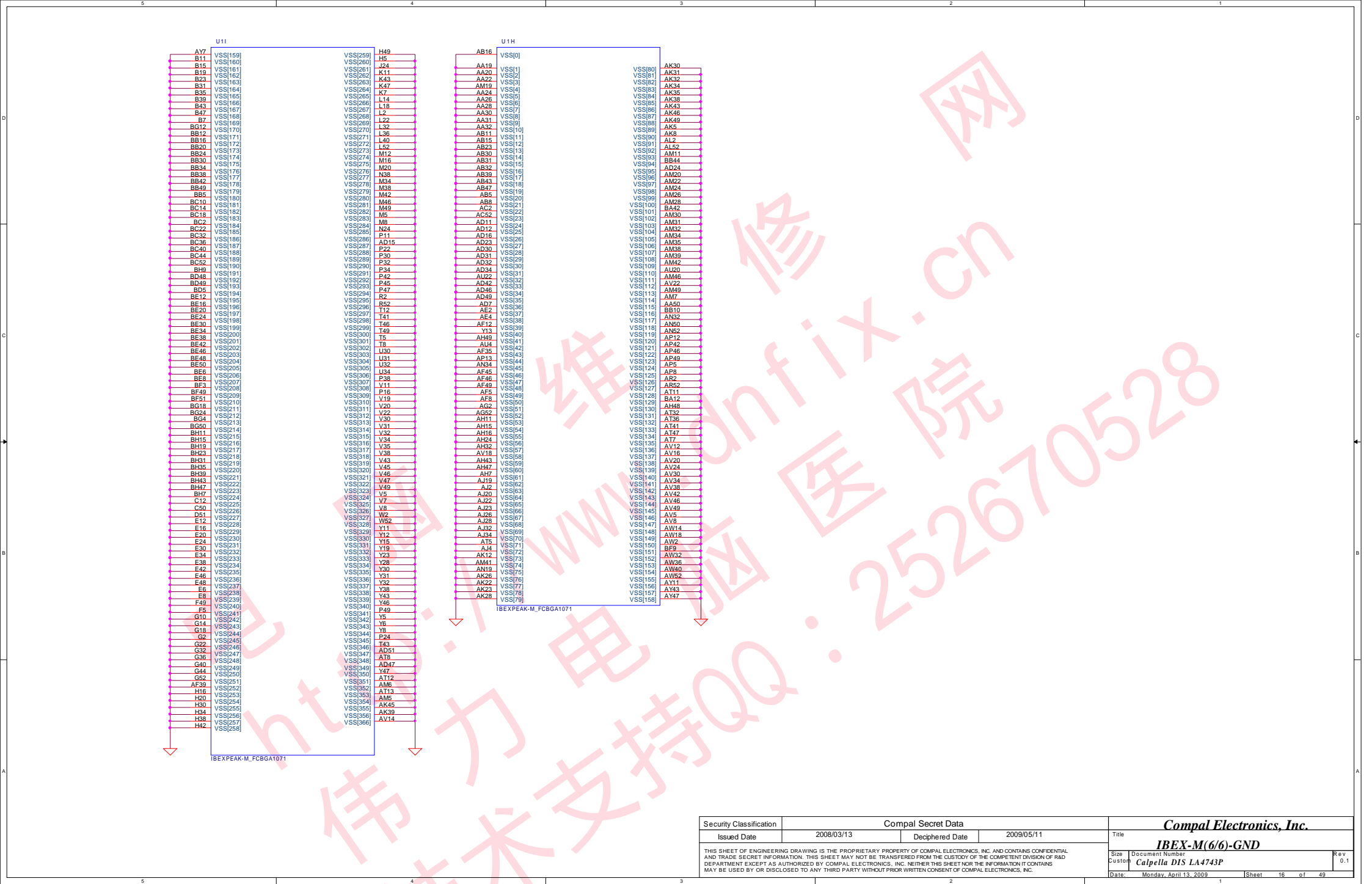


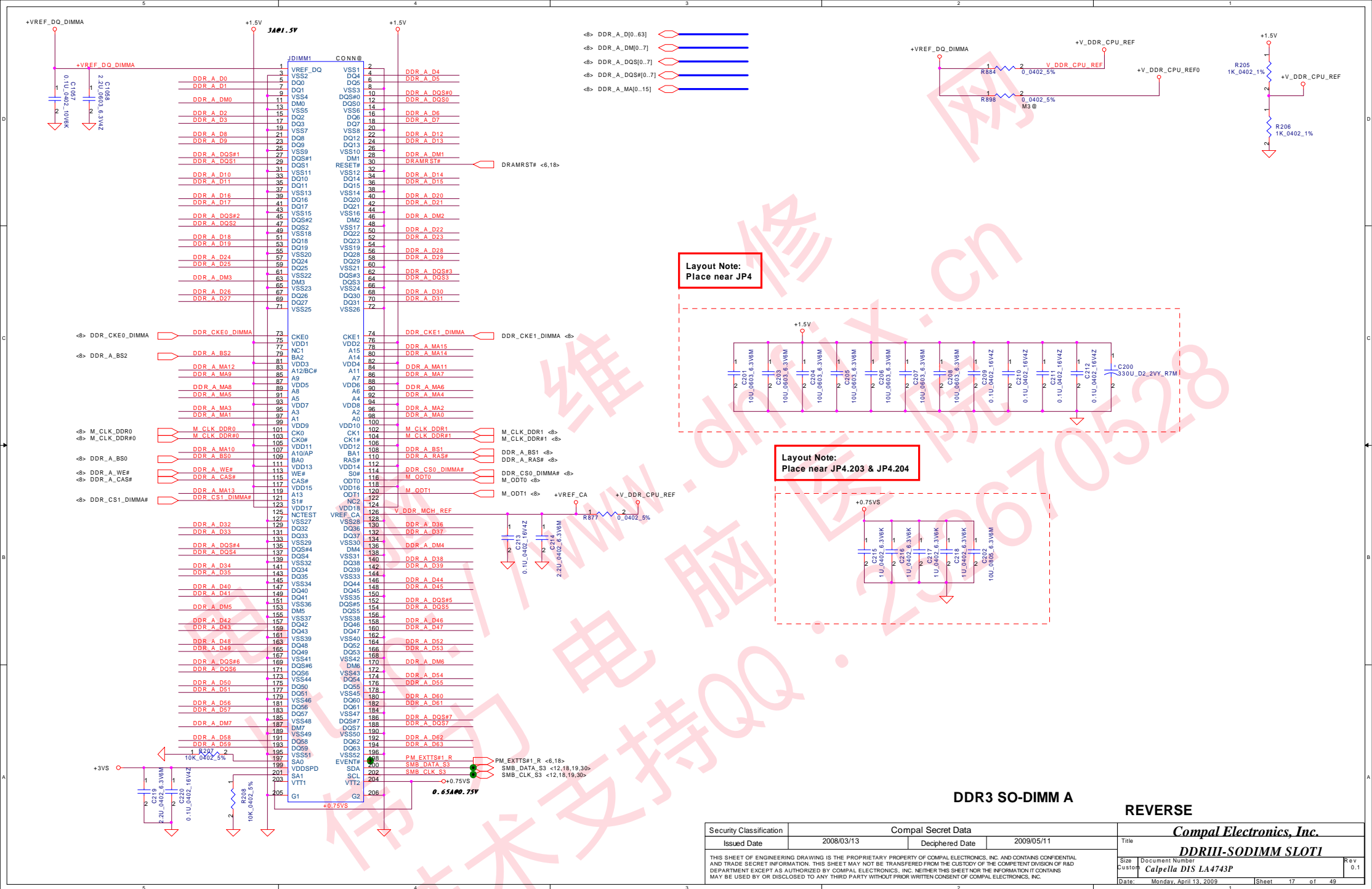




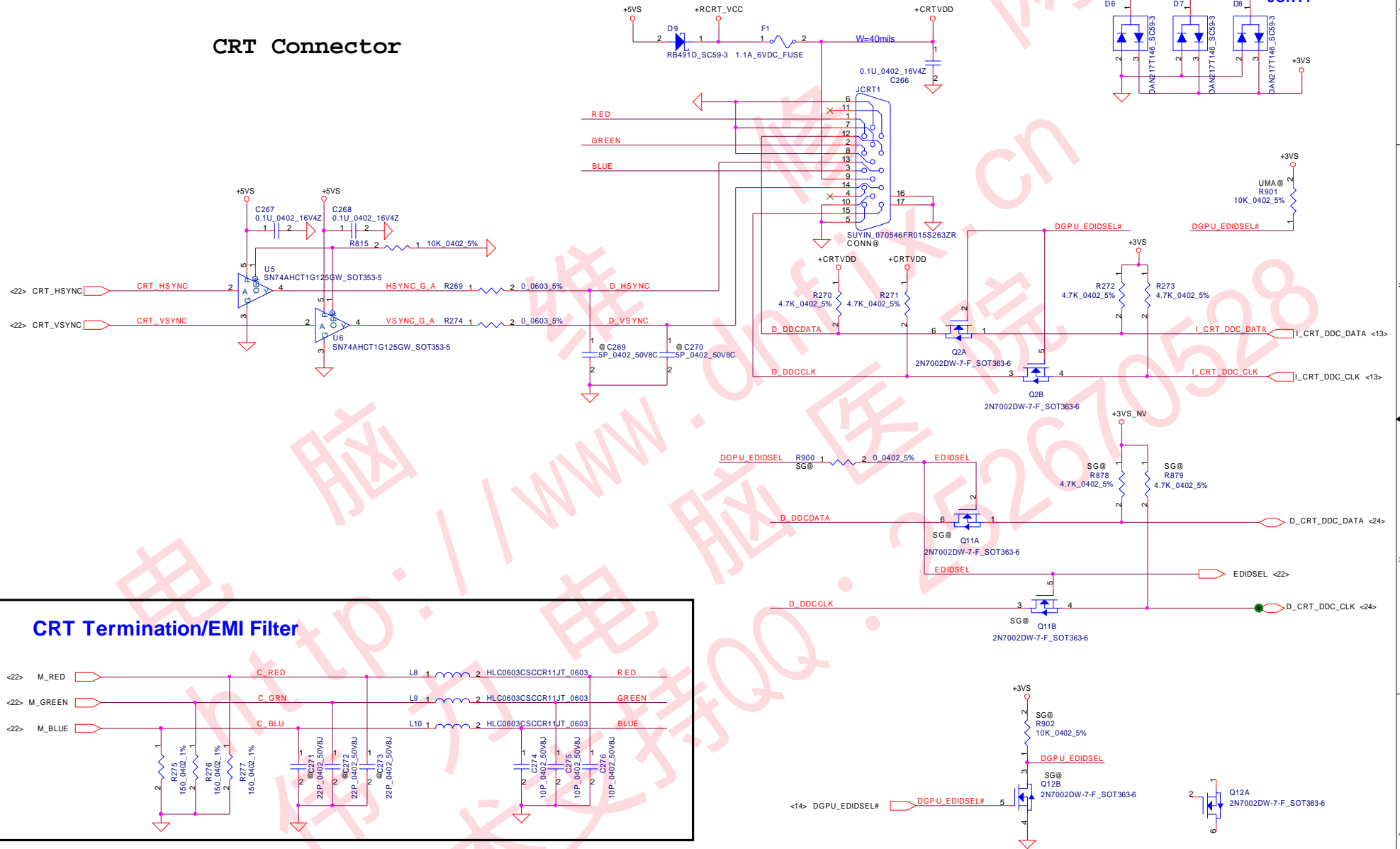


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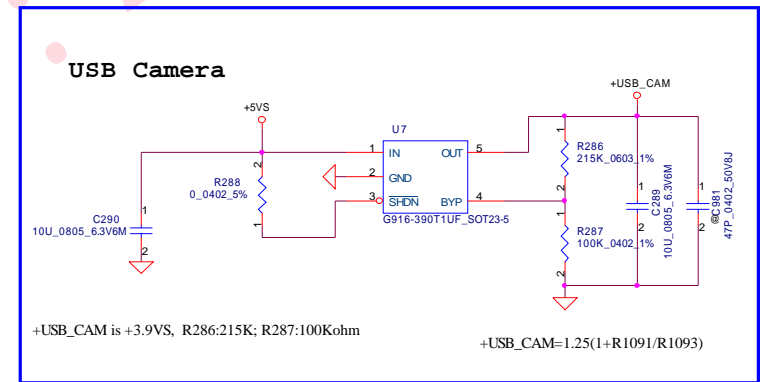
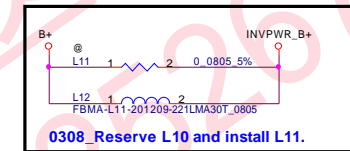
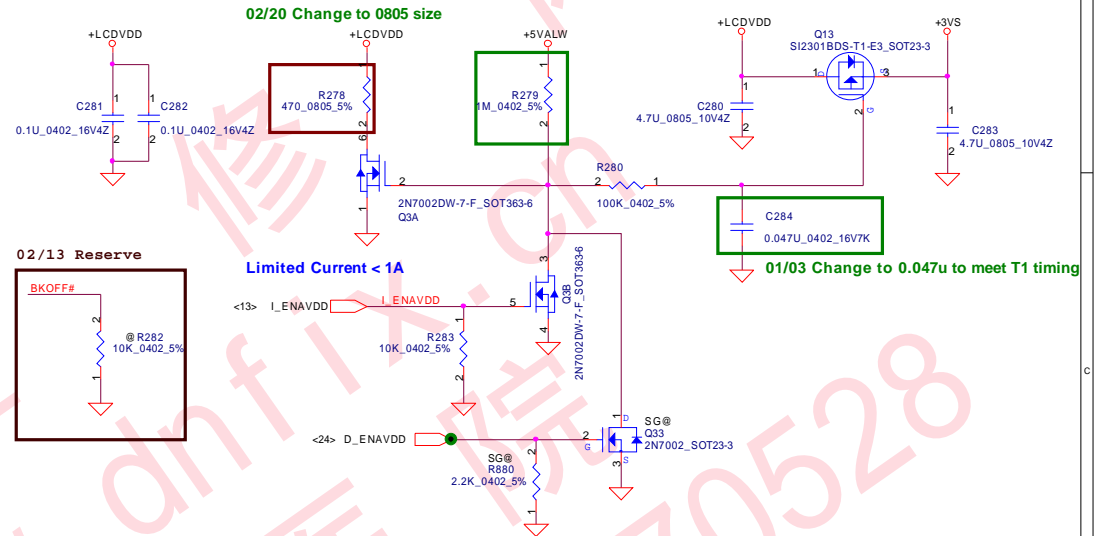
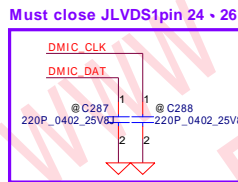
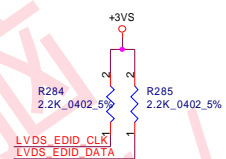
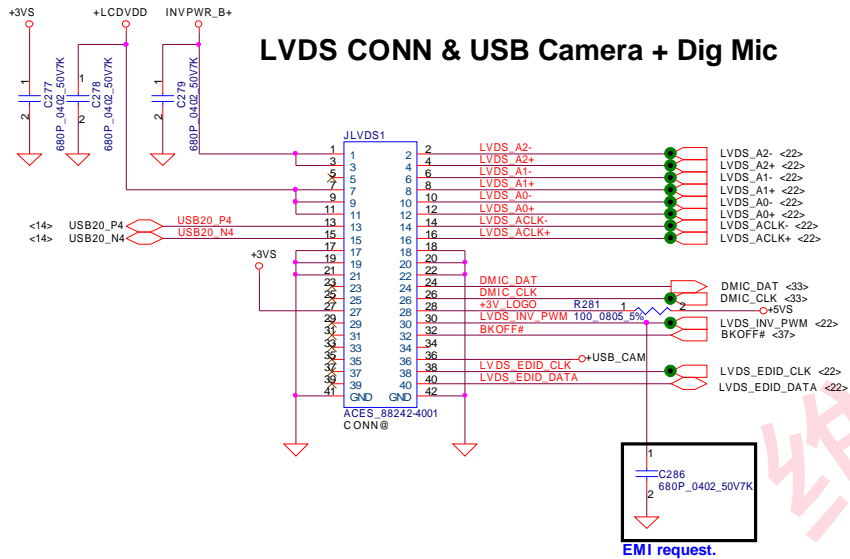




CRT Connector



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[illegible]

LVDS I2C switch

LVDS I2C switch

EDIDSEL

EDIDSEL <2>

<24> D_EDID_DATA

1 6

SG @ Q34A

2N7002DW-7-F_SOT363-B

LVDS_EDID_DATA

LVDS_ED

<13> I_EDID_DATA

R919 1 2 0.0402 5%

4 3

SG @ Q34B

2N7002DW-7-F_SOT363-B

<24> D_EDID_CLK

4 3

SG @ Q34B

2N7002DW-7-F_SOT363-B

LVDS_EDID_CLK

LVDS_EDID_CLK <21>

<13> I_EDID_CLK

R920 1 2 0.0402 5%

I LVDS_A0-	RP36	4	1	LVDS_A0-
I LVDS_A0+	3	2	2	LVDS_A0+
I LVDS_A1-	RP37	4	1	LVDS_A1-
I LVDS_A1+	3	2	2	LVDS_A1+
I LVDS_A2+	RP38	3	1	LVDS_A2+
I LVDS_A2-	4	2	2	LVDS_A2-
I LVDS_ACLK-	RP39	4	1	LVDS_ACLK-
I LVDS_ACLK+	3	2	2	LVDS_ACLK+

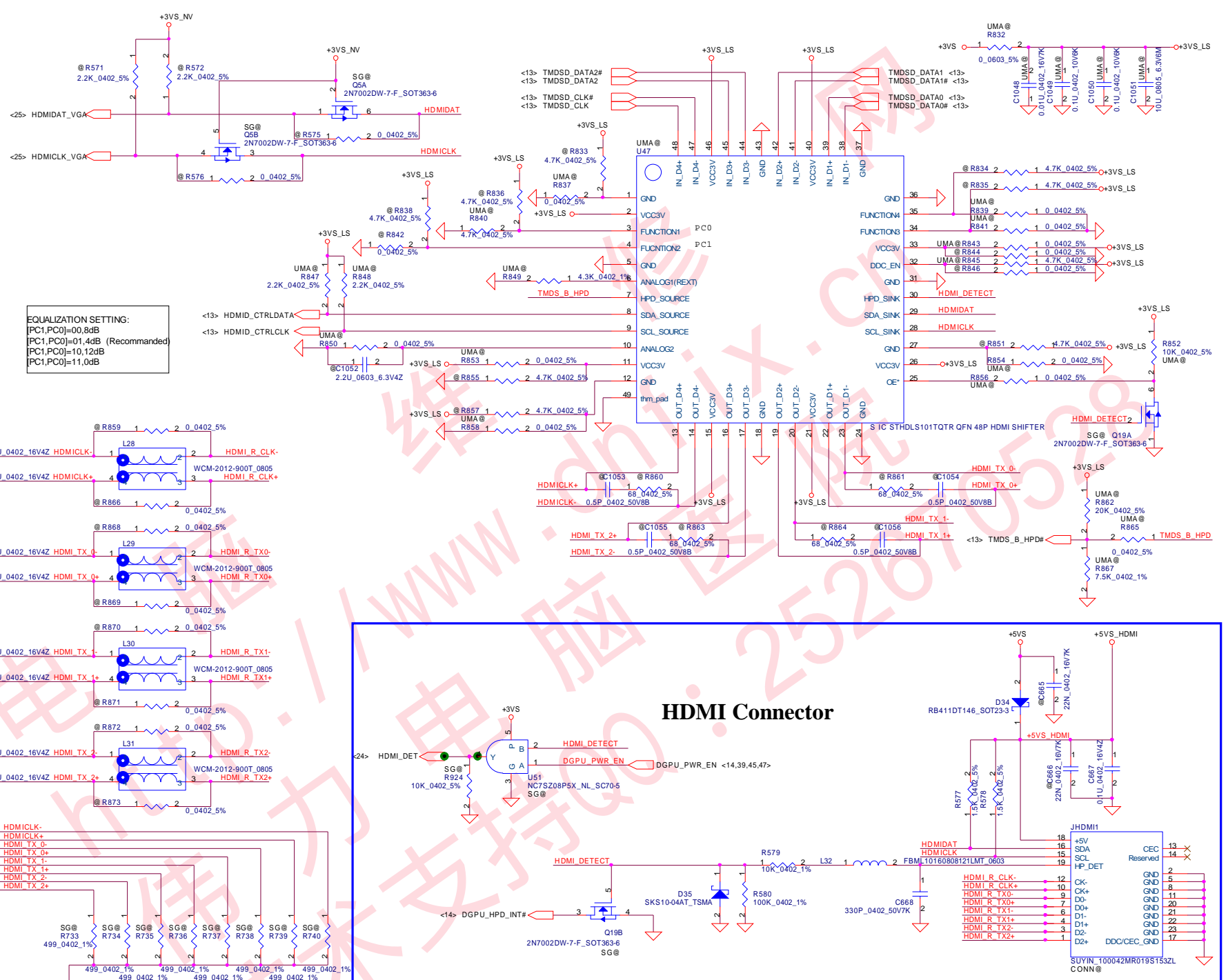
[illegible]

Pin connection diagram for the P13V512QE_GSQP24 module. The diagram shows two 24-pin connectors. The top connector (U43) has pins 1-19 connected to VDD, pins 20-23 to A0-A3, and pins 24-27 to B0-B3. The bottom connector (U44) has pins 1-19 connected to VDD, pins 20-23 to A1-A4, and pins 24-27 to B1-B4. A 3V5S voltage source is connected to pin 1 of both connectors. A DGPU_SELECT# signal is connected to pin 12 of the top connector. A CRT_HSYNCR signal is connected to pin 8 of the bottom connector. A CRT_VSYNCR signal is connected to pin 11 of the bottom connector. Ground connections are shown for pins 3, 4, 10, and 20 of the bottom connector.

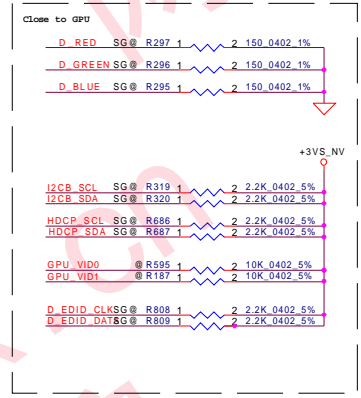
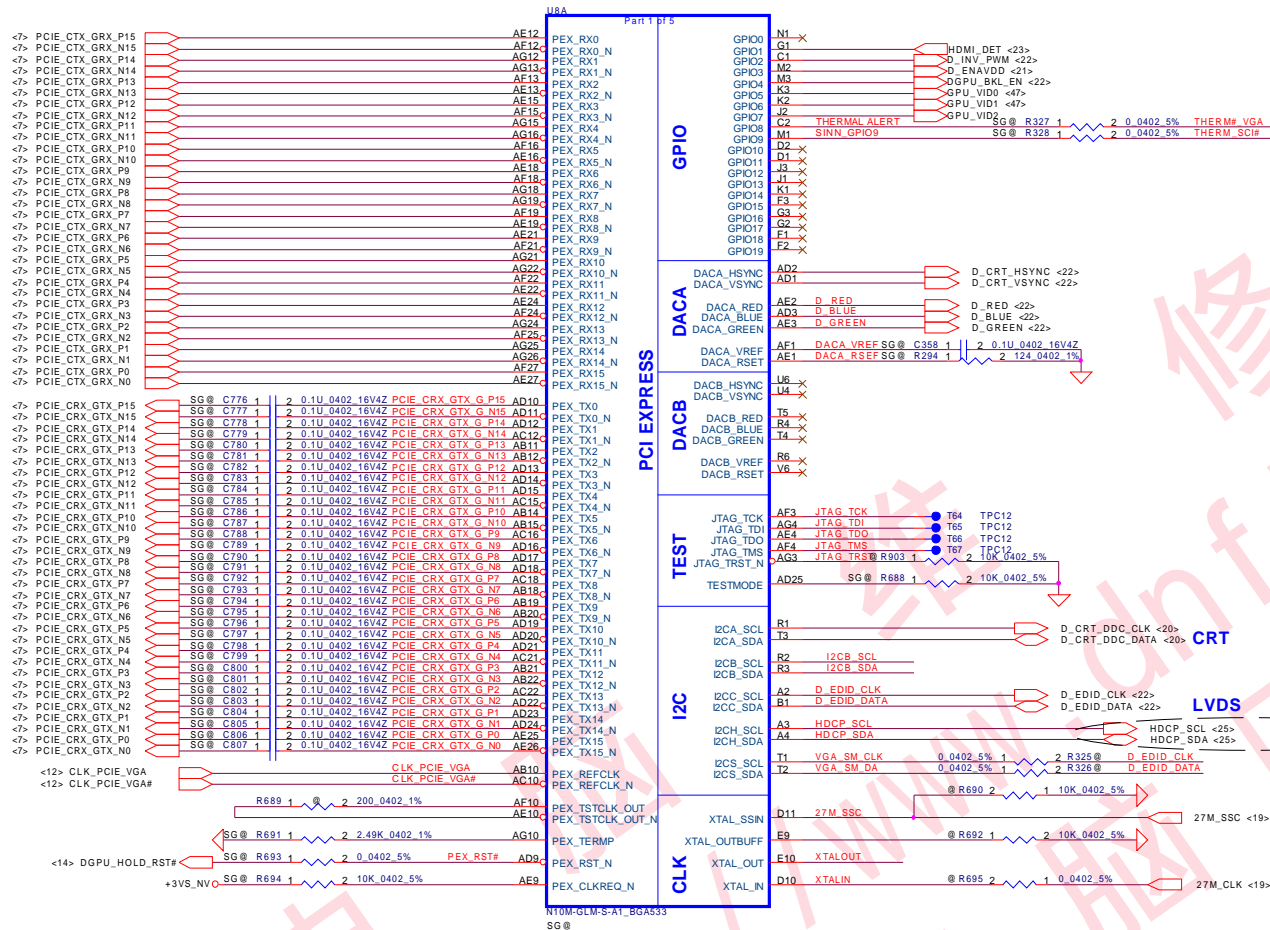
UMA ONLY (CRT)				
<u>I</u> RED	R893	2	UMA	1 0.0402.5% M RED
<u>I</u> GREEN	R894	2	UMA	1 0.0402.5% M GREEN
<u>I</u> BLUE	R895	2	UMA	1 0.0402.5% M BLUE
<u>I</u> CRT HSYNC	R896	2	UMA	1 0.0402.5% CRT HSYNC
<u>I</u> CRT VSYNC	R897	2	UMA	1 0.0402.5% CRT VSYNC

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	ST	Parade 81011	Parade 8171
R833	X	X	X
R837	0 ohm	0 ohm	4.7K ohm
R836	X	4.7K ohm	X
R840	4.7K ohm	X	4.7K ohm
R838	X	X	4.7K ohm
R842	X	X	X
R849	3.9K ohm	499 ohm	499 ohm
R850	0 ohm	X	X
C1052	X	X	2.2uF
R853	0 ohm	0 ohm	X
R855	X	X	4.7K ohm
R857	X	X	4.7K ohm
R858	0 ohm	0 ohm	X
R851	X	X	4.7K ohm
R854	0 ohm	0 ohm	X
R843	0 ohm	0 ohm	X
R844	X	X	4.7K ohm
R839	0 ohm	X	4.7K ohm
R834	X	X	X
R841	0 ohm	X	X
R835	X	X	4.7K ohm
C667	0.1uF	1uF	1uF
R862	V	X	X
R867	V	X	X

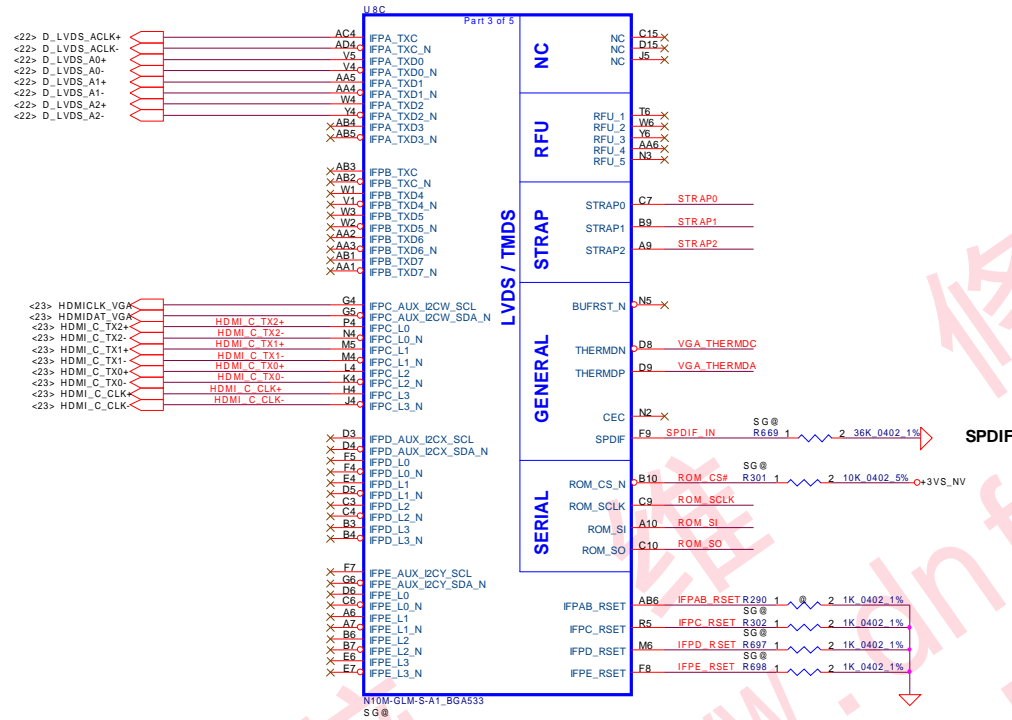


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				Size Document Number		Rev
				Custom Calpella D1S LA473P		0.1
Date:		Monday, April 13, 2009		Sheet	23 of 49	

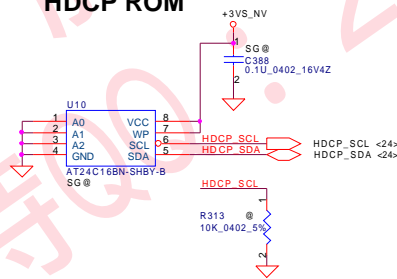


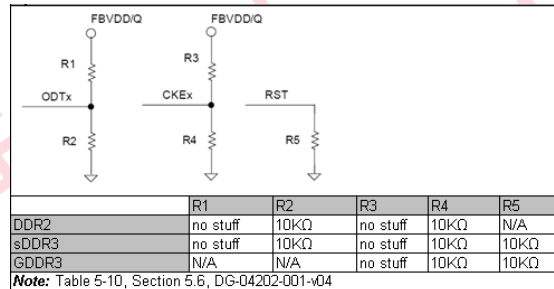
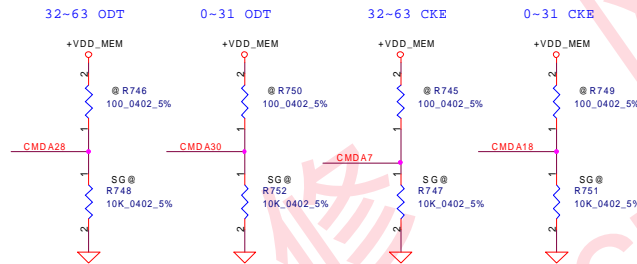
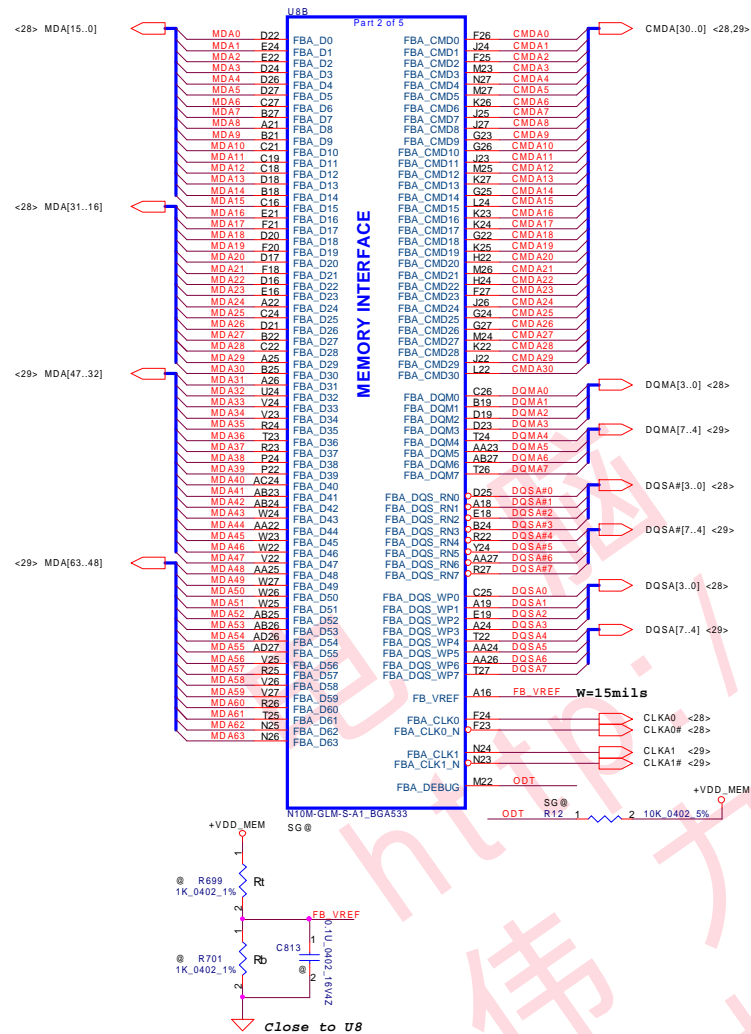
GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	HPD-C (used for IFPC)
GPIO1	IN	N/A	2nd DVI Hot-plug
GPIO2	OUT	H	Panel Back-Light PWM
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light Enable
GPIO5	OUT	N/A	NVDD VID0
GPIO6	OUT	N/A	NVDD VID1
GPIO7	OUT	N/A	NVDD VID2
GPIO8	IN	L	OVERT
GPIO9	OUT	L	Thermal Alert
GPIO10	OUT	N/A	MEM_VREF
GPIO11	OUT	L	SLI SYNCO
GPIO12	IN	N/A	AC Detect
GPIO13	OUT	L	MEM_VID
GPIO14	OUT	H	PS Control
GPIO15	IN	N/A	HPD-E (used for IFPE)
GPIO16	OUT	N/A	FAN PWM Control
GPIO17		N/A	
GPIO18		N/A	
GPIO19	IN	N/A	HPD-D (used for IFPD)

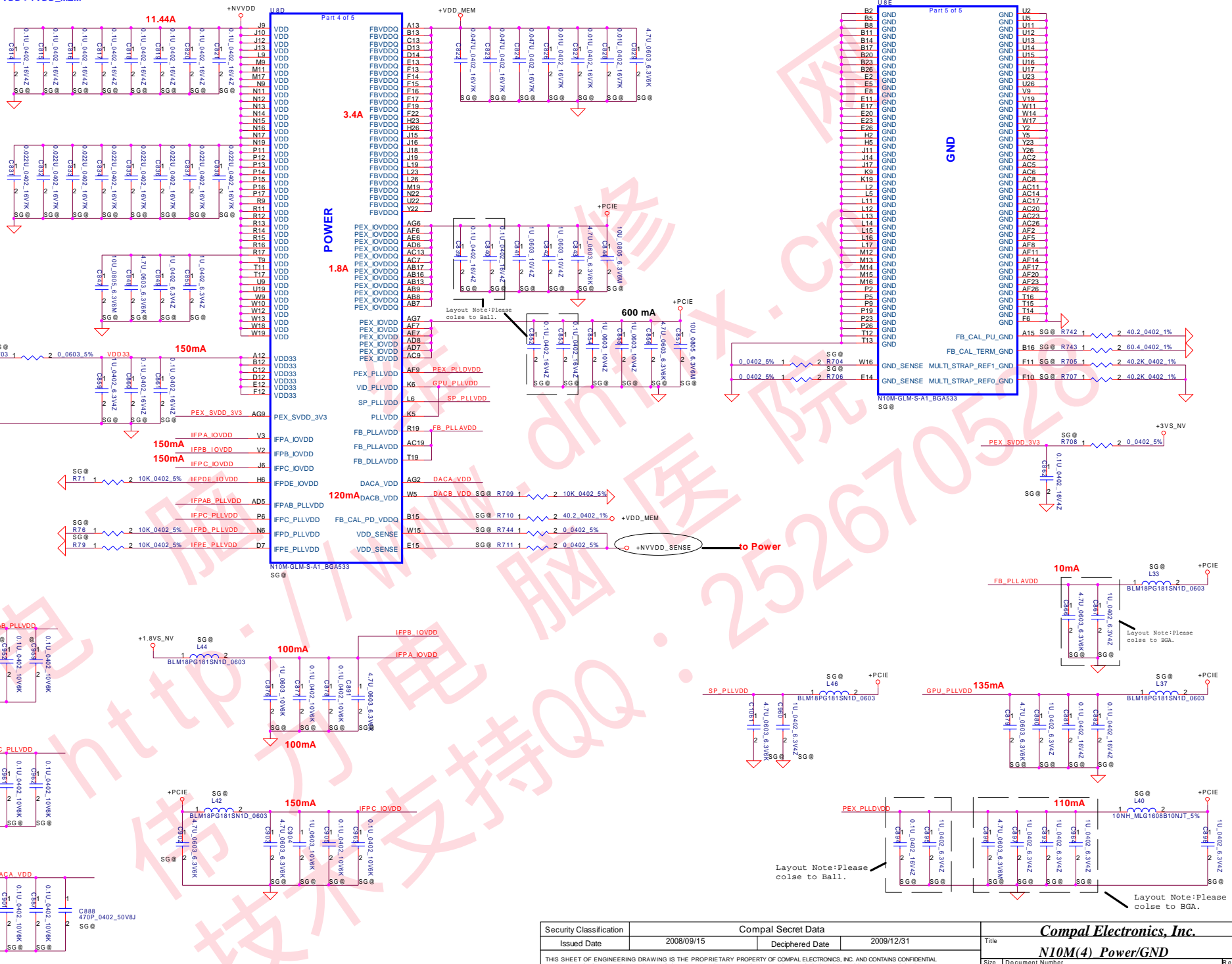
LVDS Interface



HDCP ROM



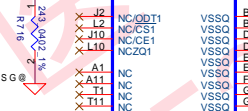
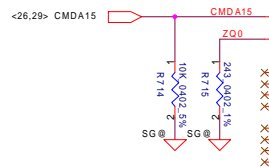




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				Size	Document Number
				Customer	Calpella DTS LA473P Date: Monday, April 13, 2009
				Sheet	27 of 49

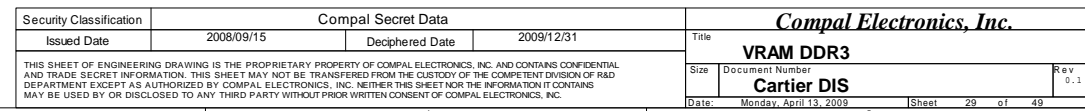
Low 32 bit FB

Hynix : H5TQ1G63BFR-12C-->SA000032400
Samsung : K4W1G1646E-HC12-->SA000035700

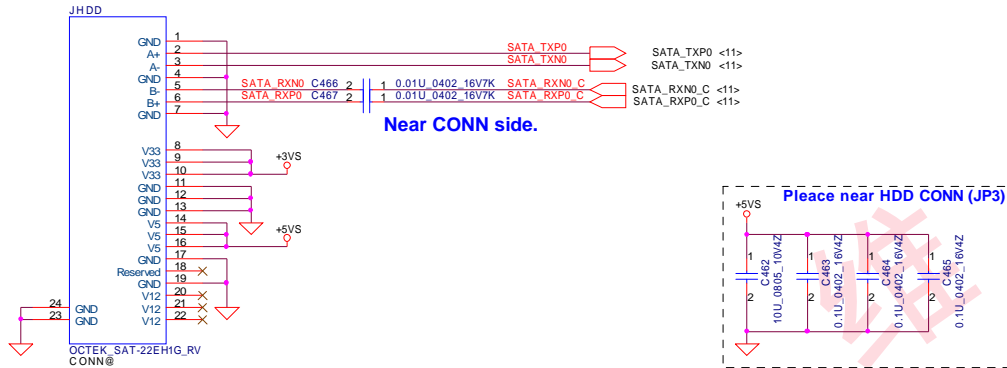


LOW HIGH

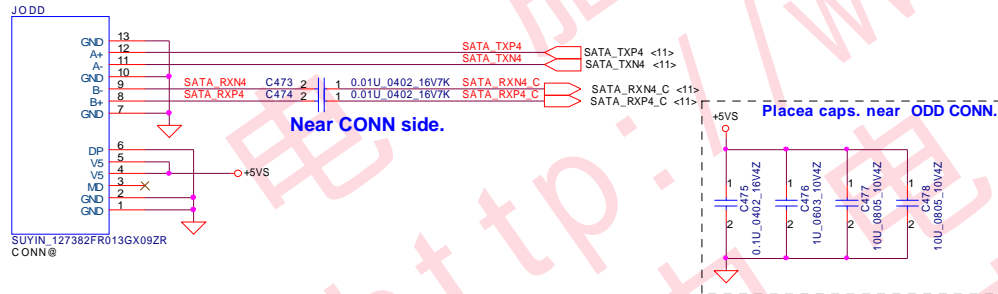
High 32 bit FB



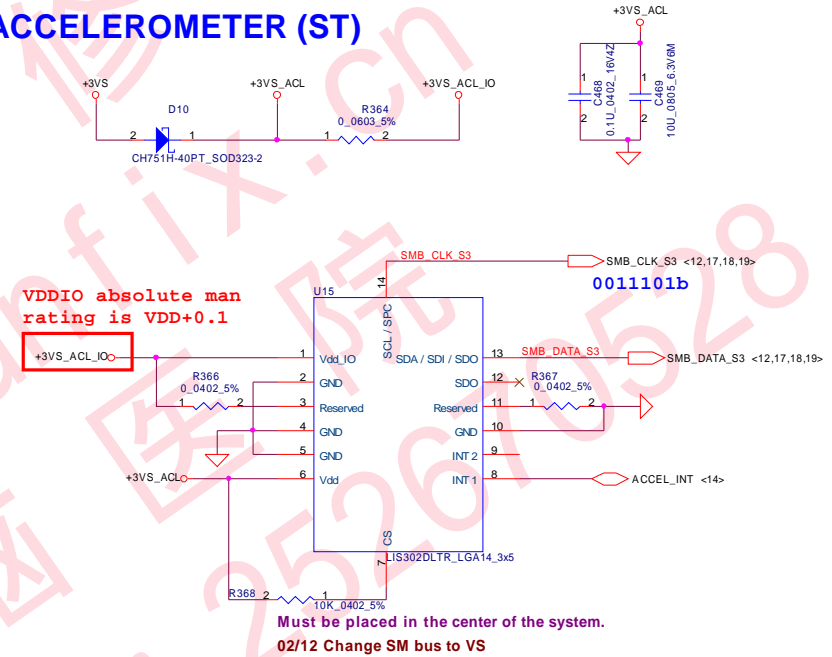
HDD Connector



CD-ROM Connector

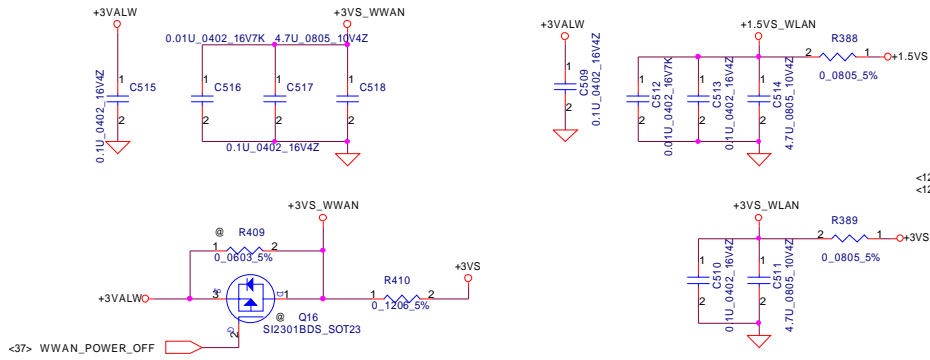


ACCELEROMETER (ST)

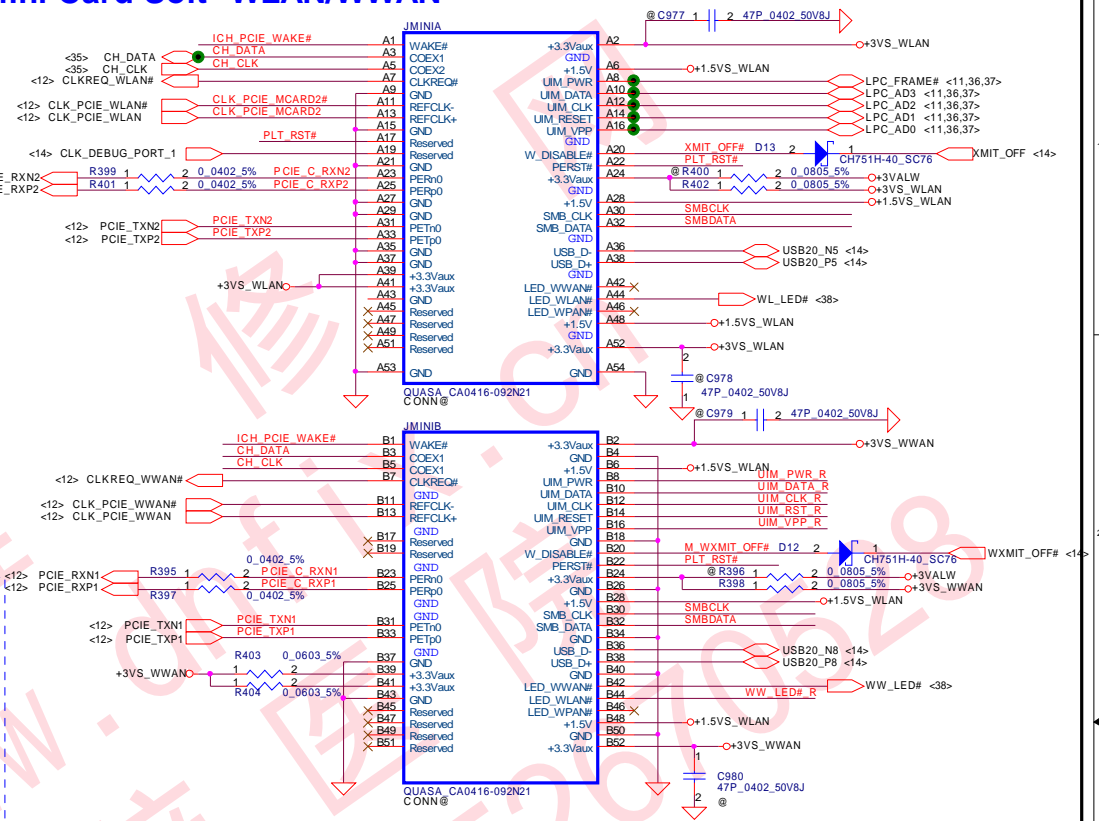
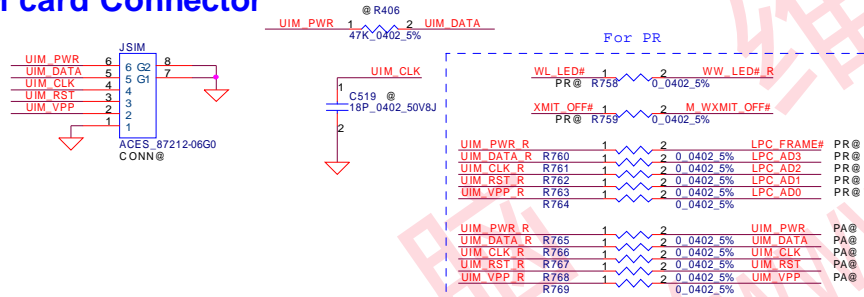


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Mini Card Solt--WLAN/WWAN

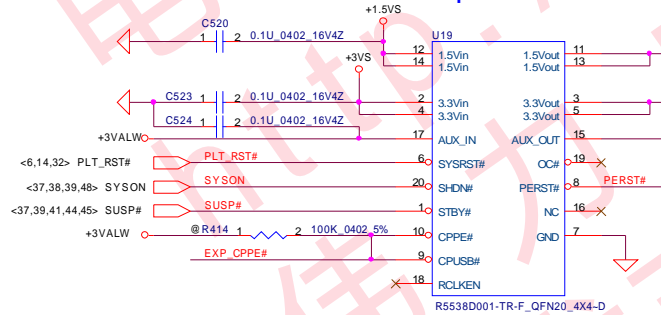


SIM card Connector

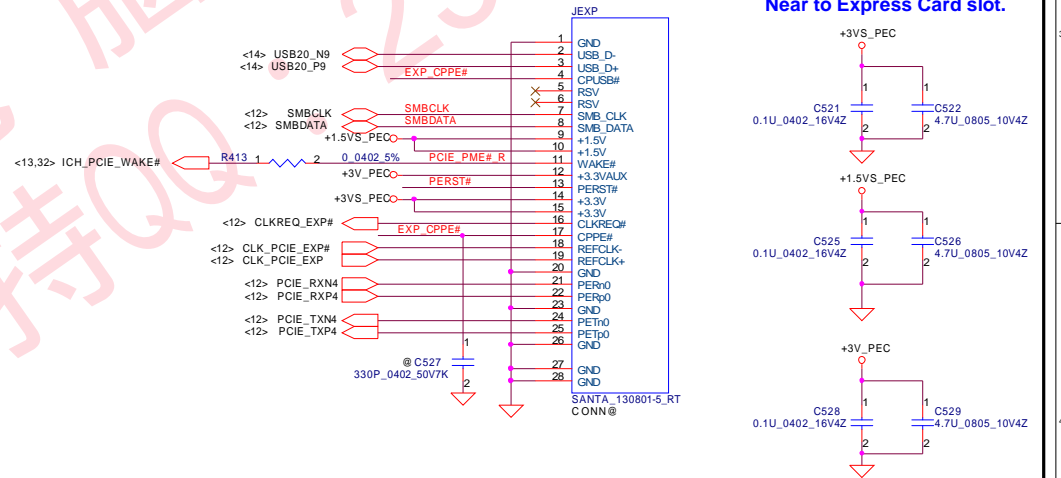


New Card

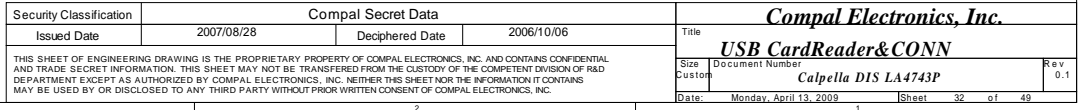
Express Card Power Switch

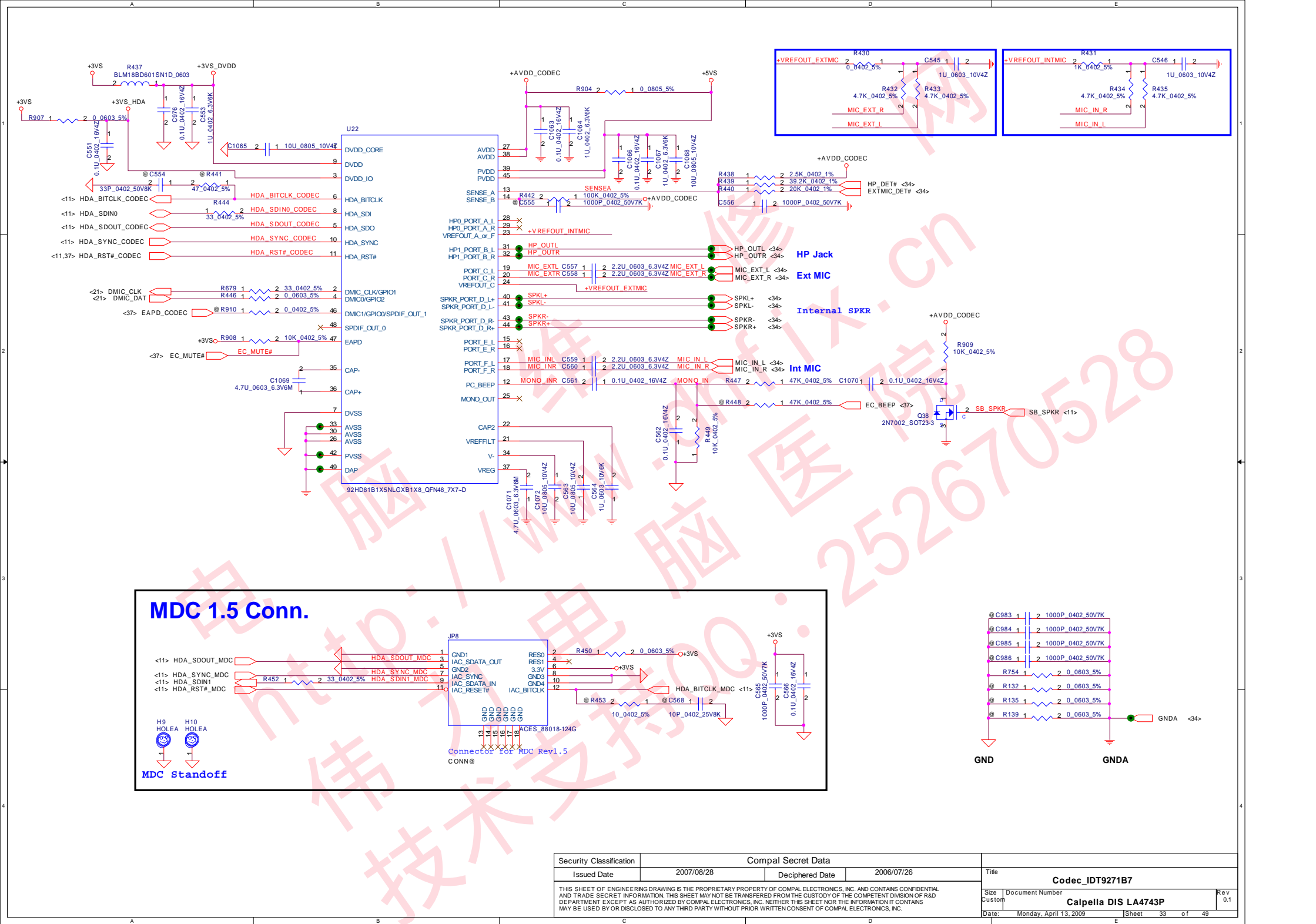


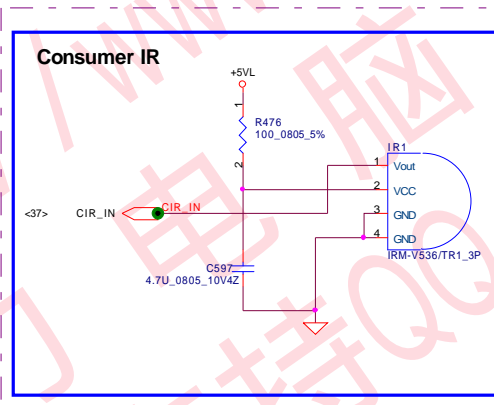
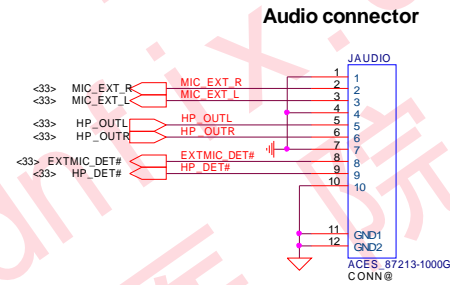
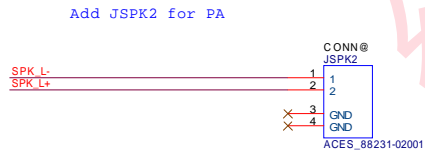
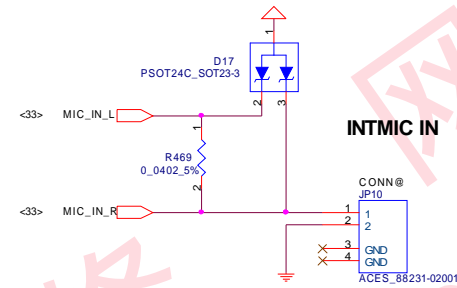
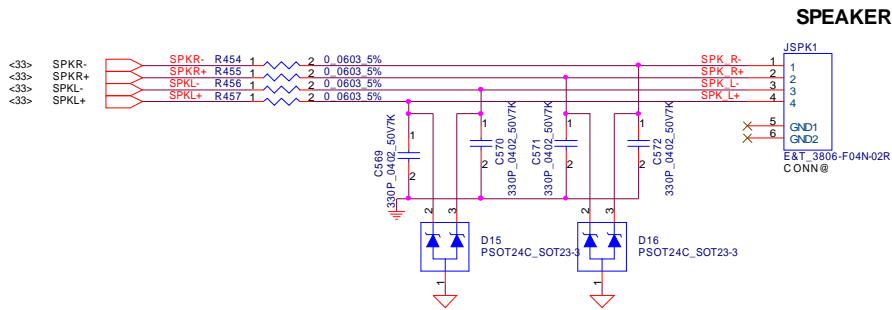
internal pull high to 3.3Vaux-in
EC need setting at Hi-Z & output Low



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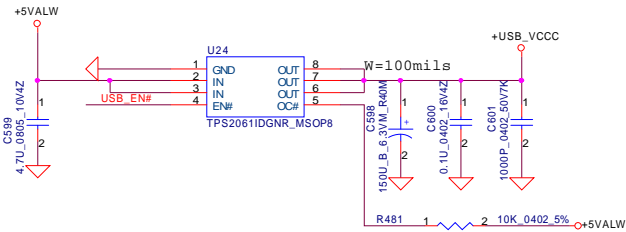




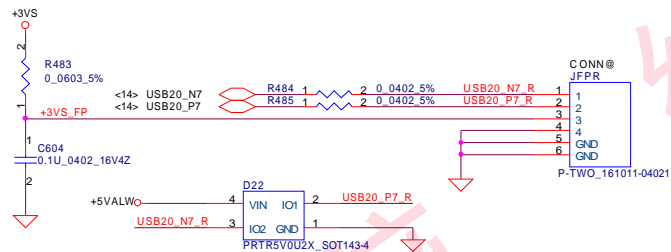


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2006/07/26				2006/07/26				2006/07/26			
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34				of				49			
Rev				0.1				Calpella DIS LA4743P			

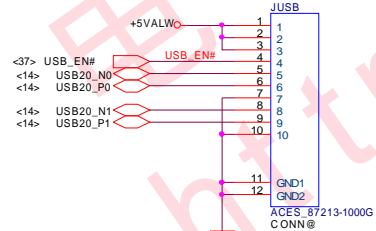
Right side USB Power Switch



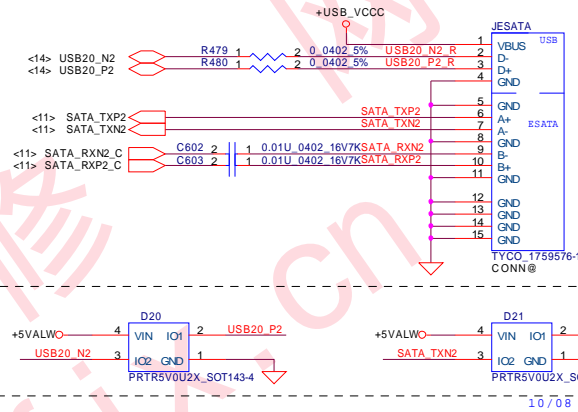
Finger printer



USB cable connector for Left side

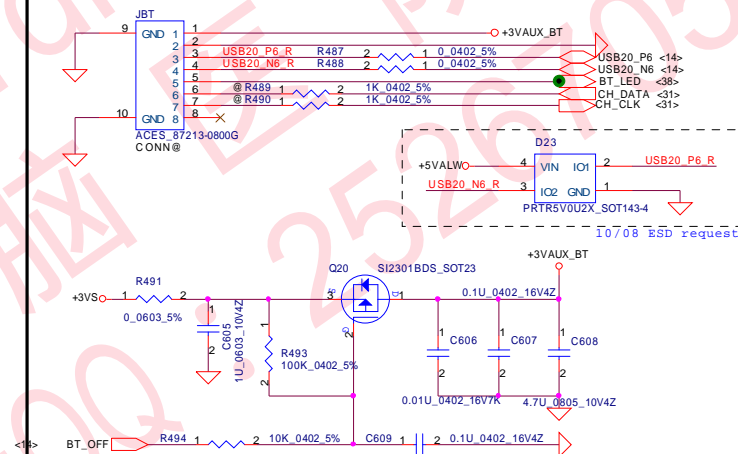


Right side ESATA/USB combination Connector



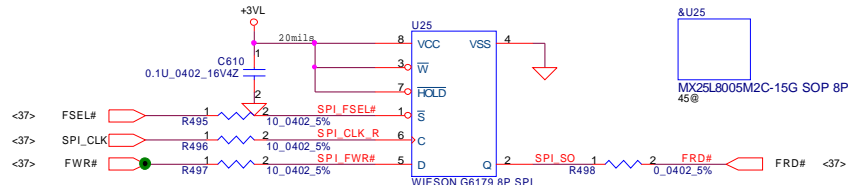
BT Connector

Need change to New version



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SPI ROM => 1M (EC code)



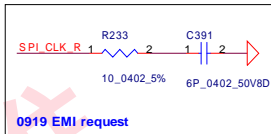
SP07000F500 S SOCKET WIESON G6179-100000 8P SPIFLASH
WIESO_G6179-100000_8P

SA00000XT00 : S IC FL 8M MX25L8005M2C-15G SOP 8P (MXIC)

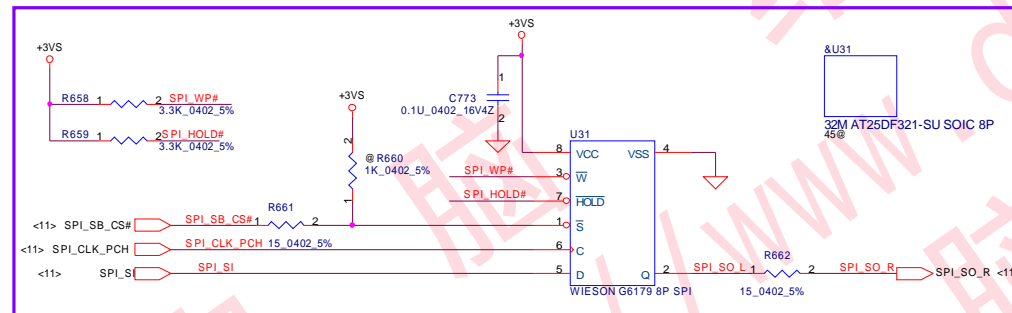
SA00001AW00 : S IC FL 16M MX25L1605AM2C-15G SOP 8P SPI (MXIC)

SA000021A00 : S IC FL 32M MX25L3205DM2I-12G SOP 8P (MXIC)

SA000031Q00 : S IC FL 32M AT25DF321-SU SOIC 8P (ATMEL)

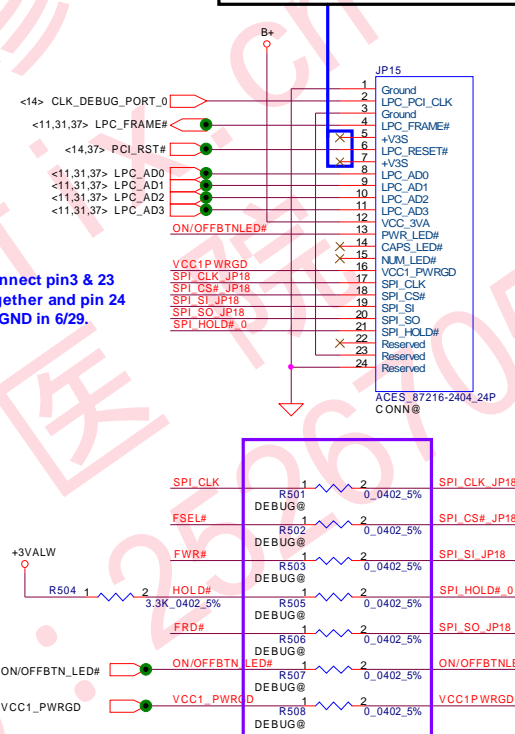


SPI ROM on PCH => 4M (ME code + System BIOS)



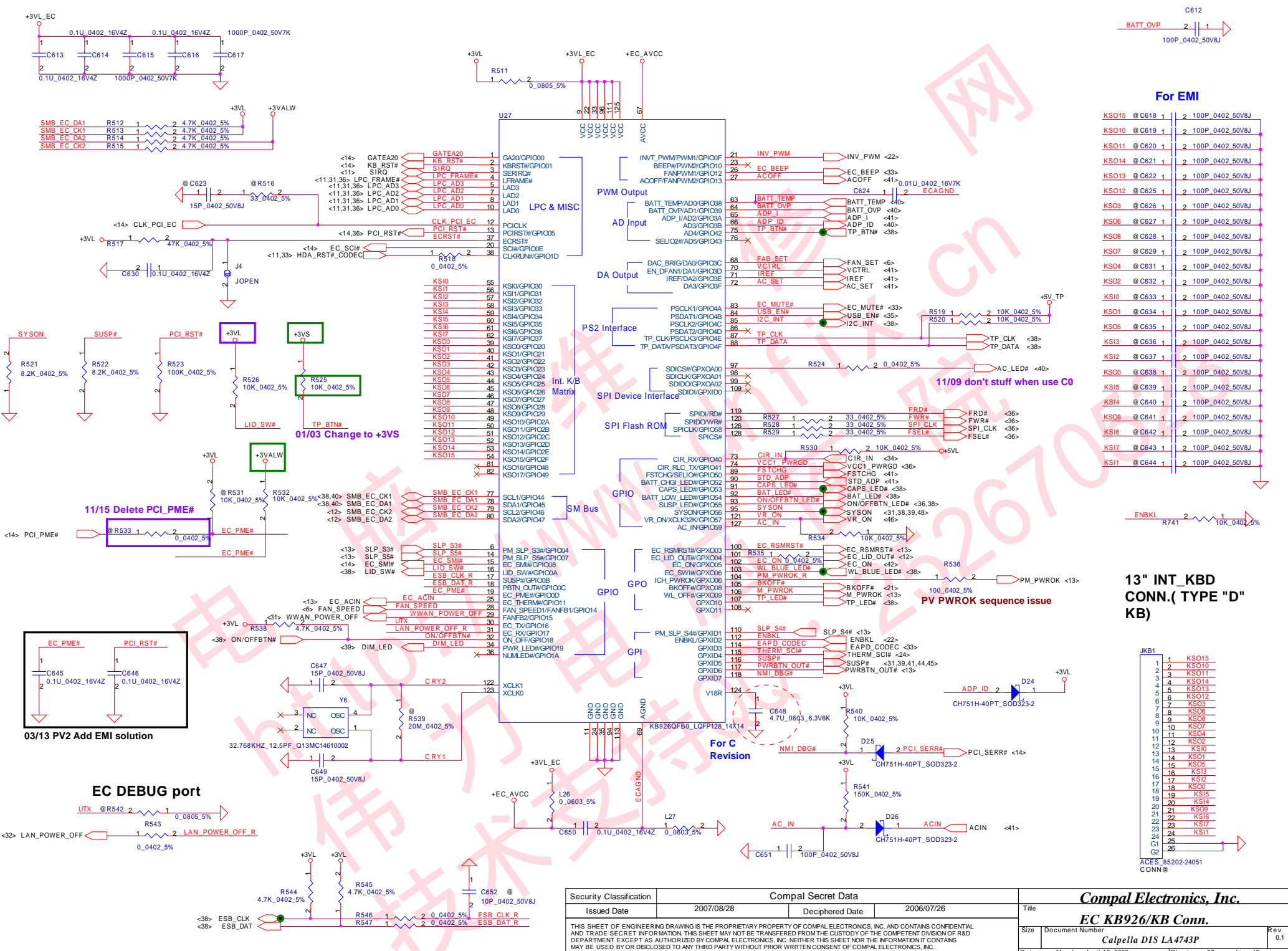
LPC Debug Port

Change from +3VL to +3VS. 6/9
Removed +3VS. 6/13



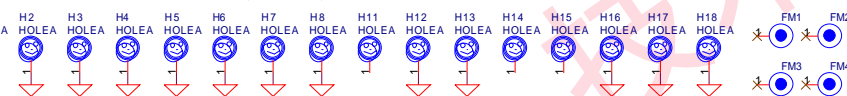
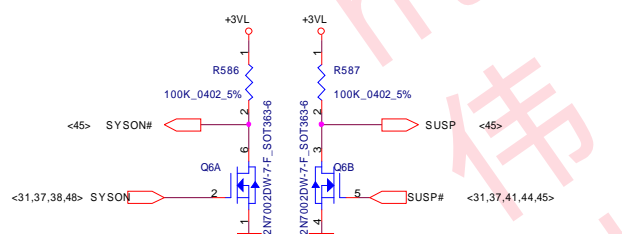
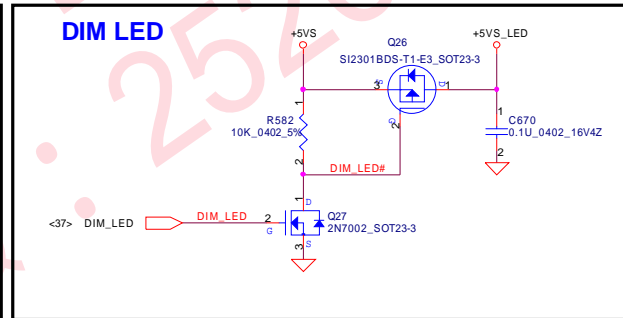
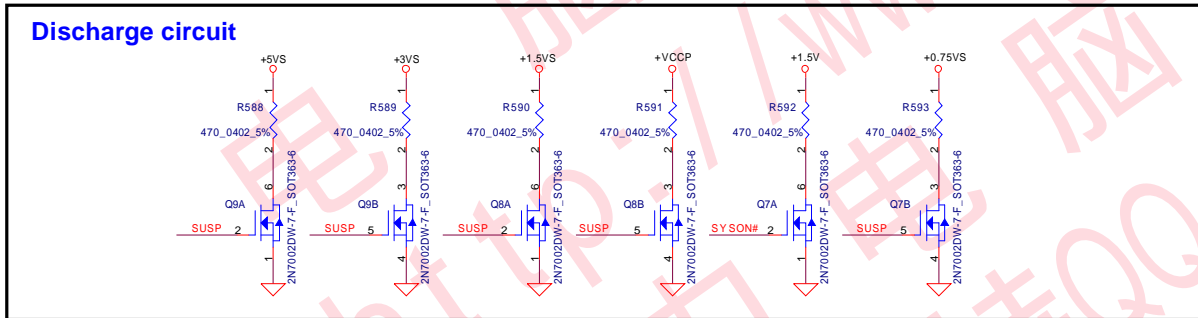
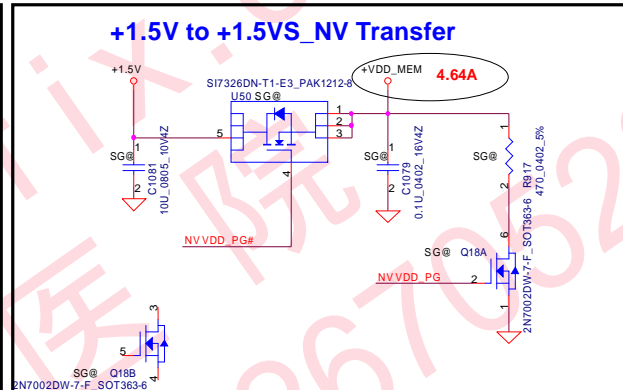
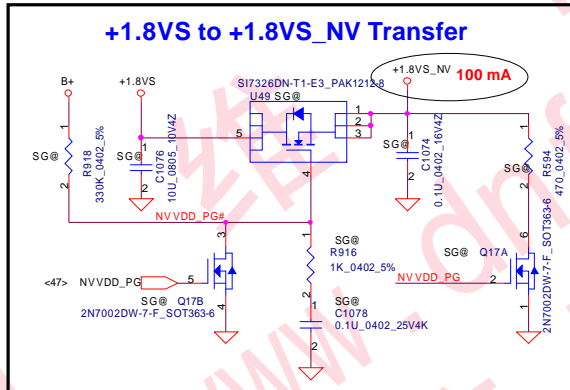
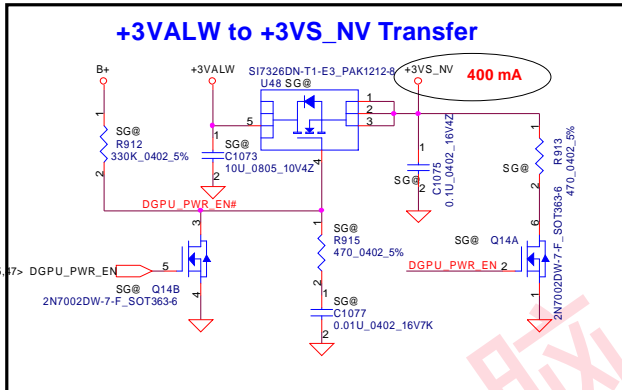
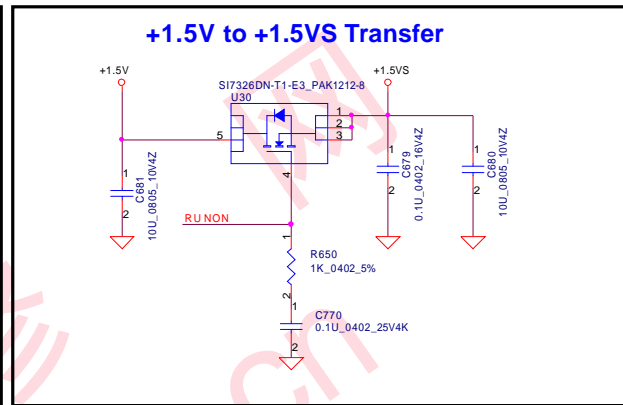
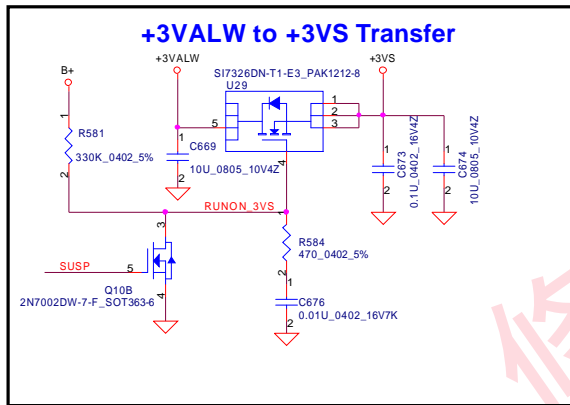
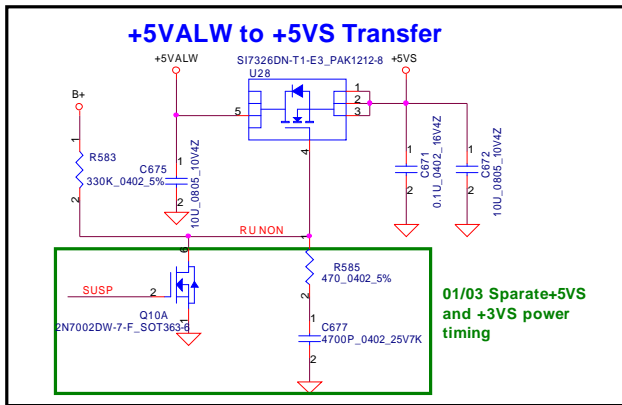
11/07 Add 0 Ohm for debug port

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								Calpella DIS LA4743P			
								Rev 0.1			
				Date				Monday, April 13, 2009			
								Sheet 36 of 49			

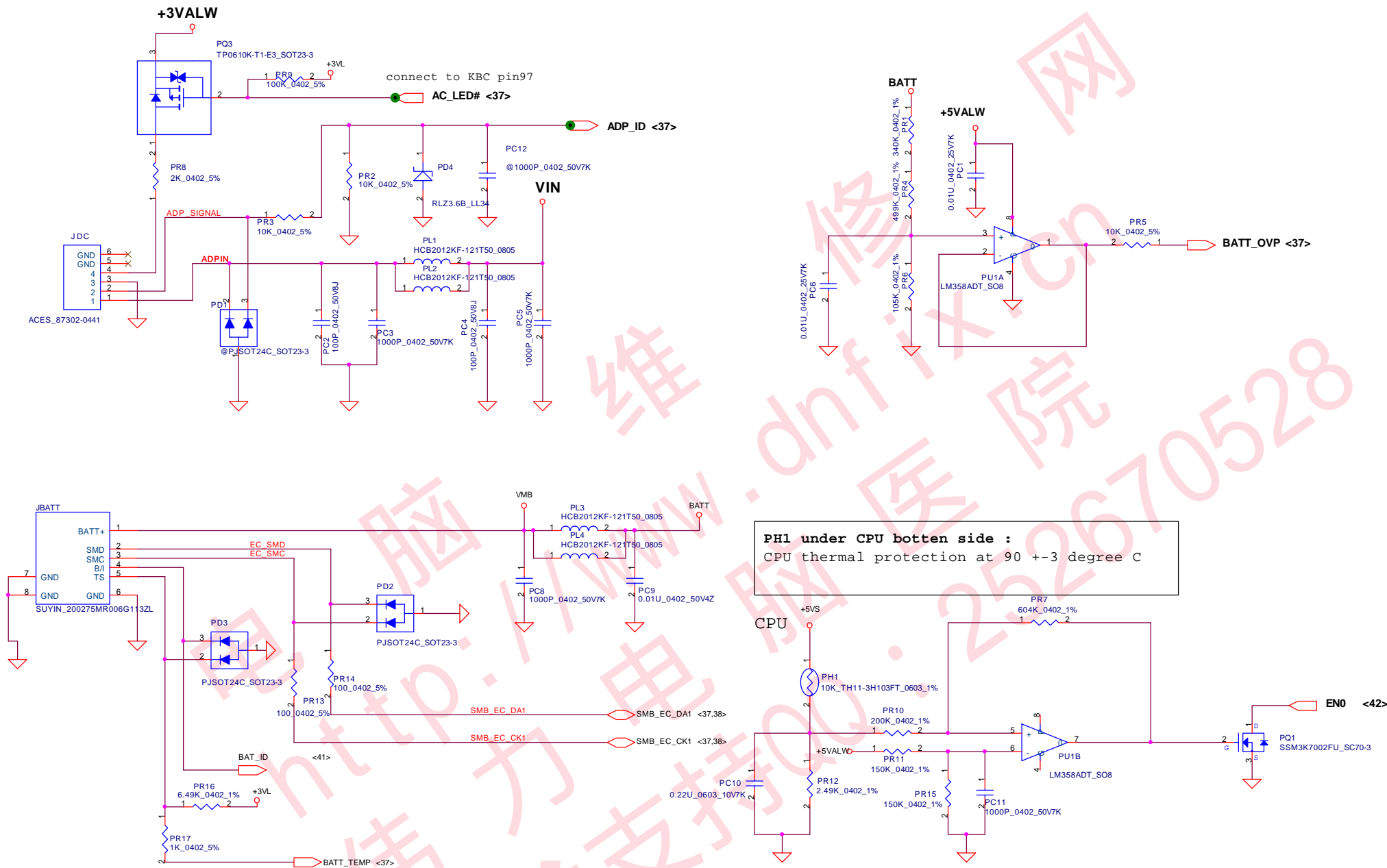


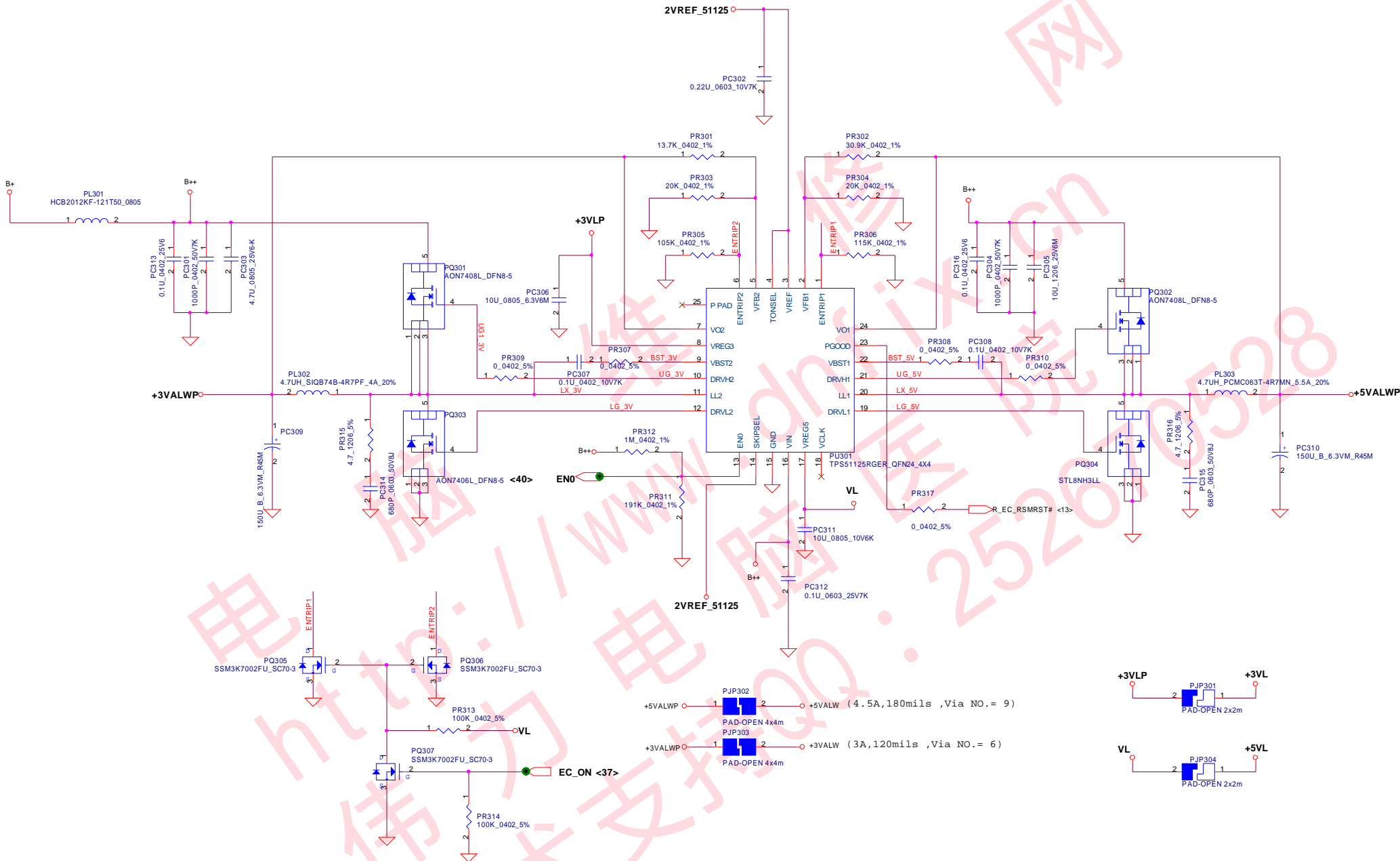
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					Calpella DIS LA4743P	0.1
				Date:	Monday, April 13, 2009	Sheet 38 of 49

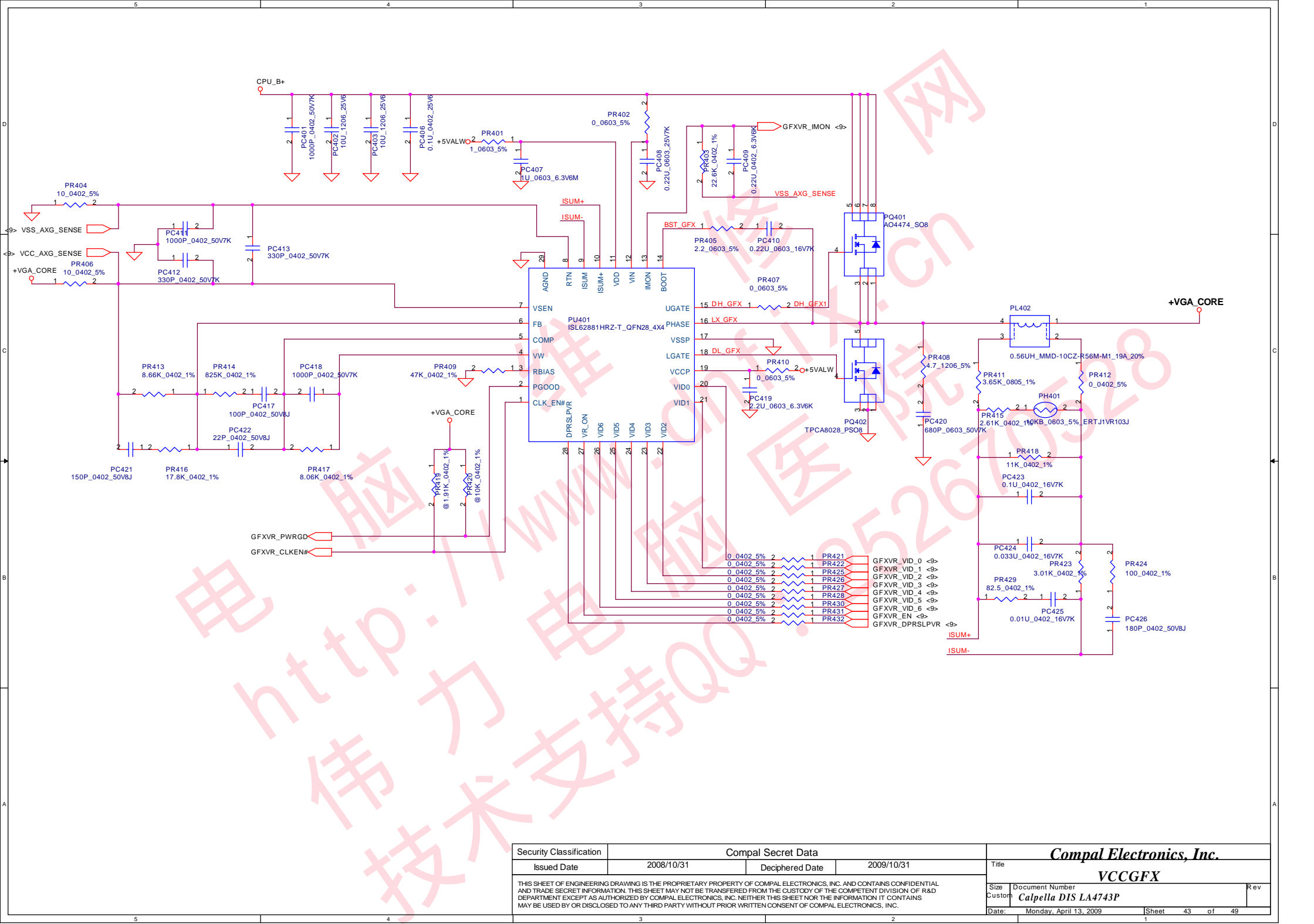


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				Calpella DIS LA4743P	
				Date:	Monday, April 13, 2009
				Sheet	39 of 49

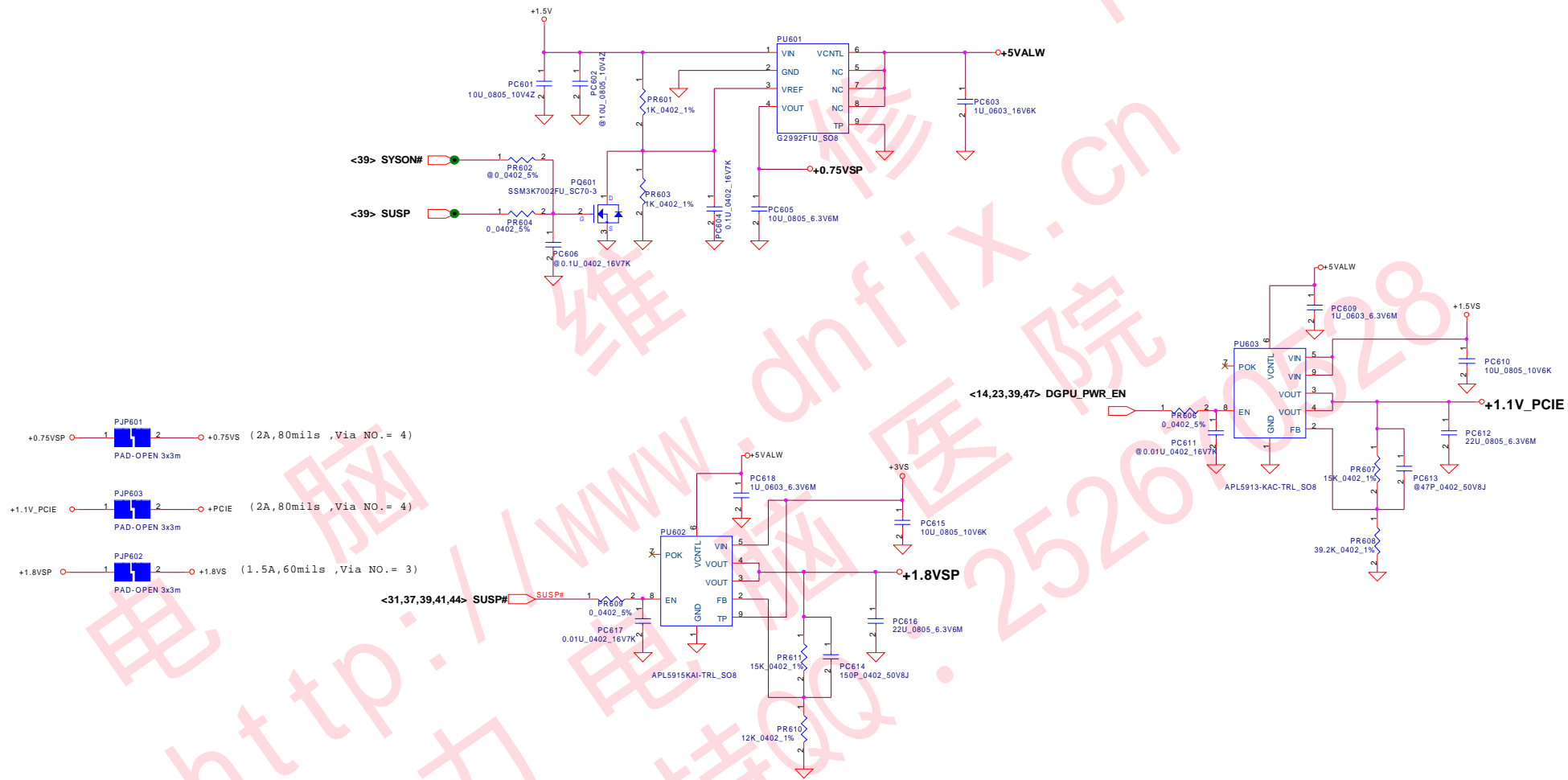




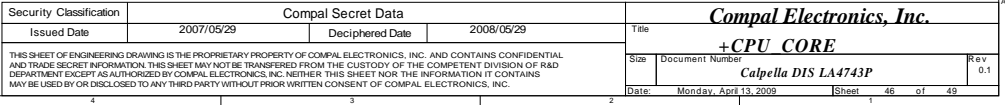
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				Size		
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				Custom		
				Calpella DIS LA4743P		
				Date:	Monday, April 13, 2009	Sheet 42 of 49
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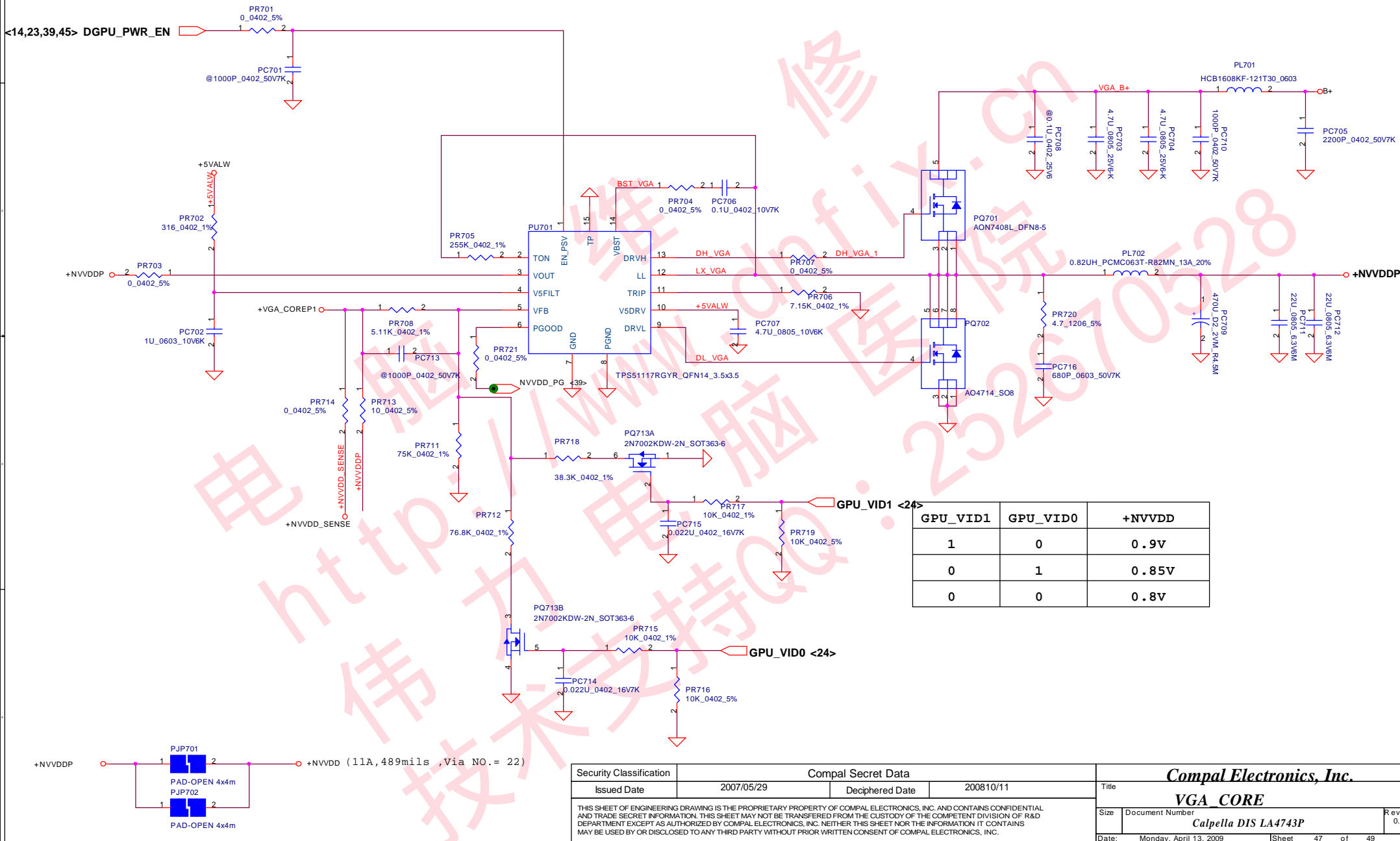


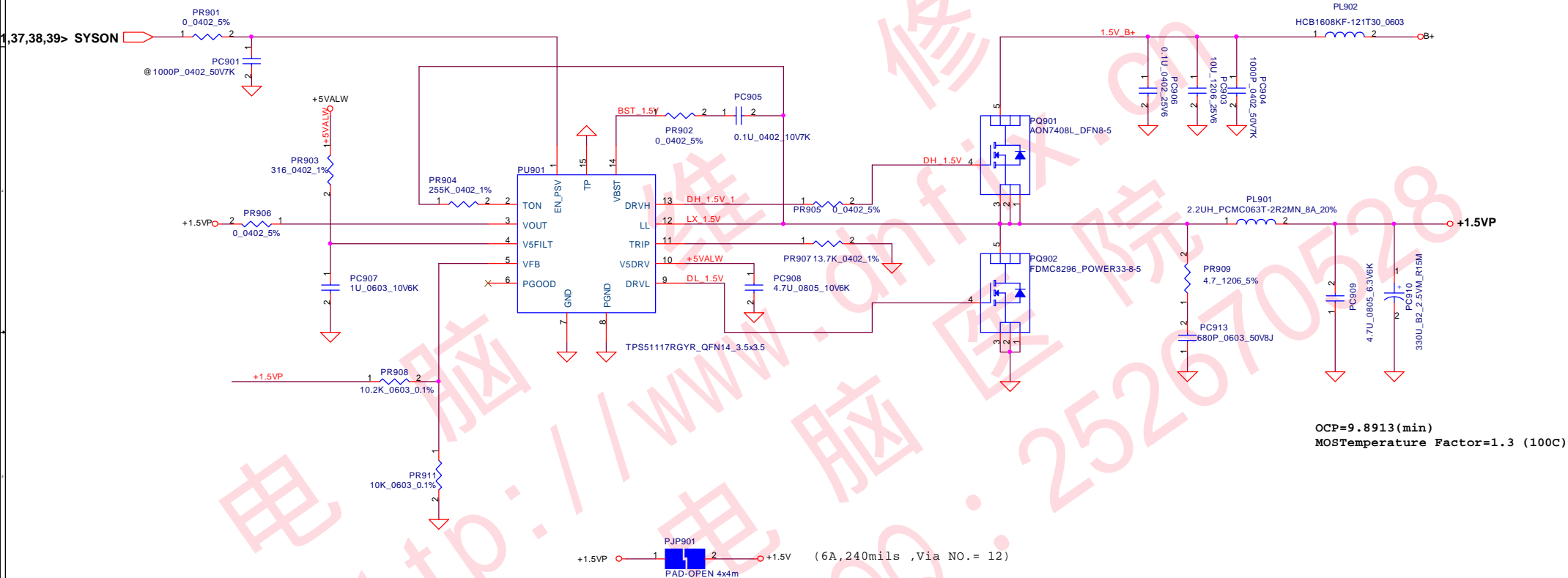
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Version Change List (P. I. R. List) for Power Circuit

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